

Compal Confidential

HCL51 Schematics Document

Intel Yonah Processor with ATIRC410MD/E + DDRII + SB460M

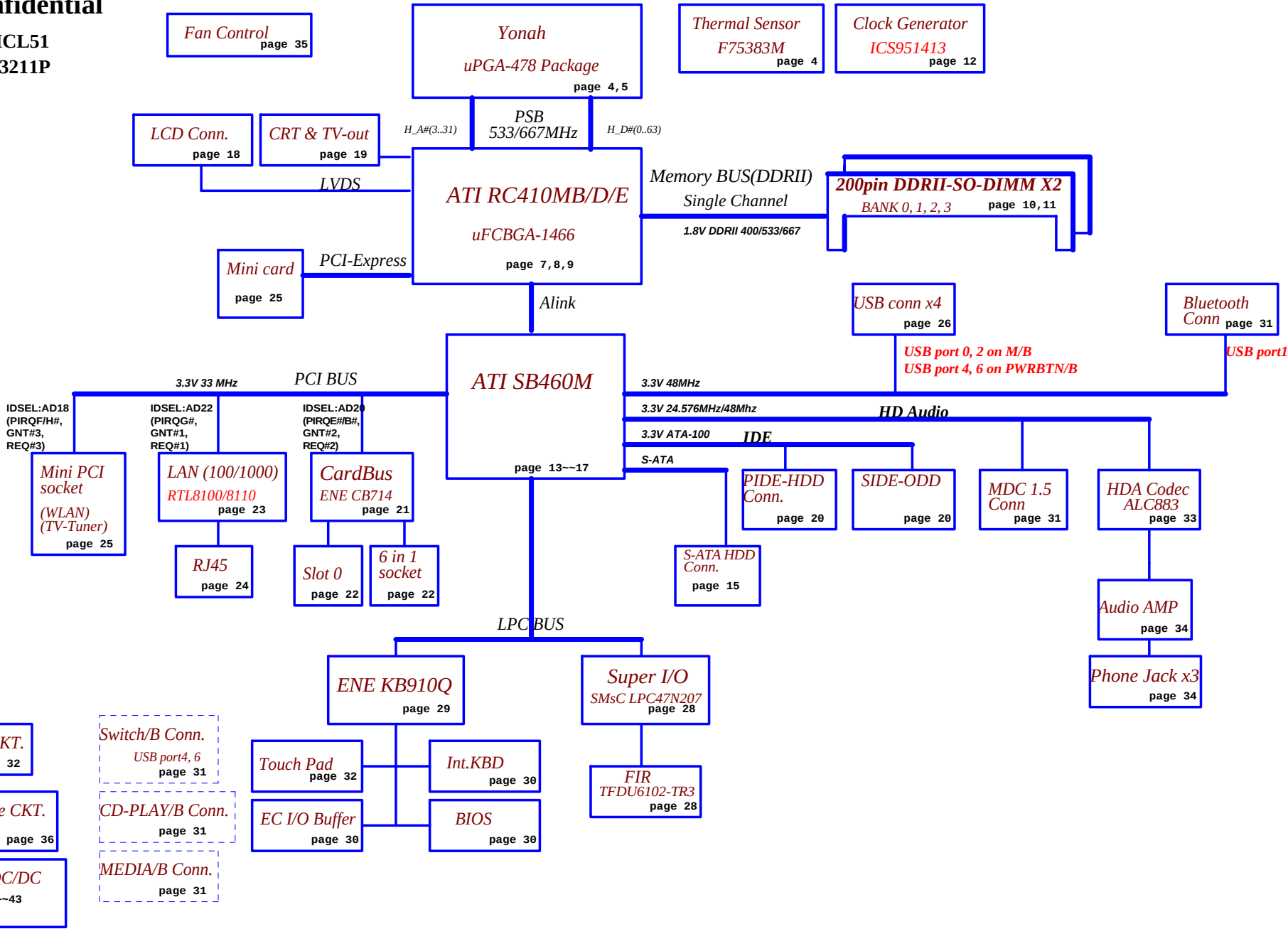
2006-04-05

REV: 1.0

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Model Name : HCL51
File Name : LA-3211P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTC/VCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQE/PIRQH
1394	AD16	0	PIRQA
LAN(10/100)	AD22	1	PIRQG
Mini-PCI(WLAN/TV-Tuner)	AD18	3	PIRQF/PORQH

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Fintek F75383M	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

EC SM Bus2 address

SB460M SM Bus address

Device	Address
Clock Generator (ICS951413)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	0.2
2	0.2
3	
4	
5	
6	
7	

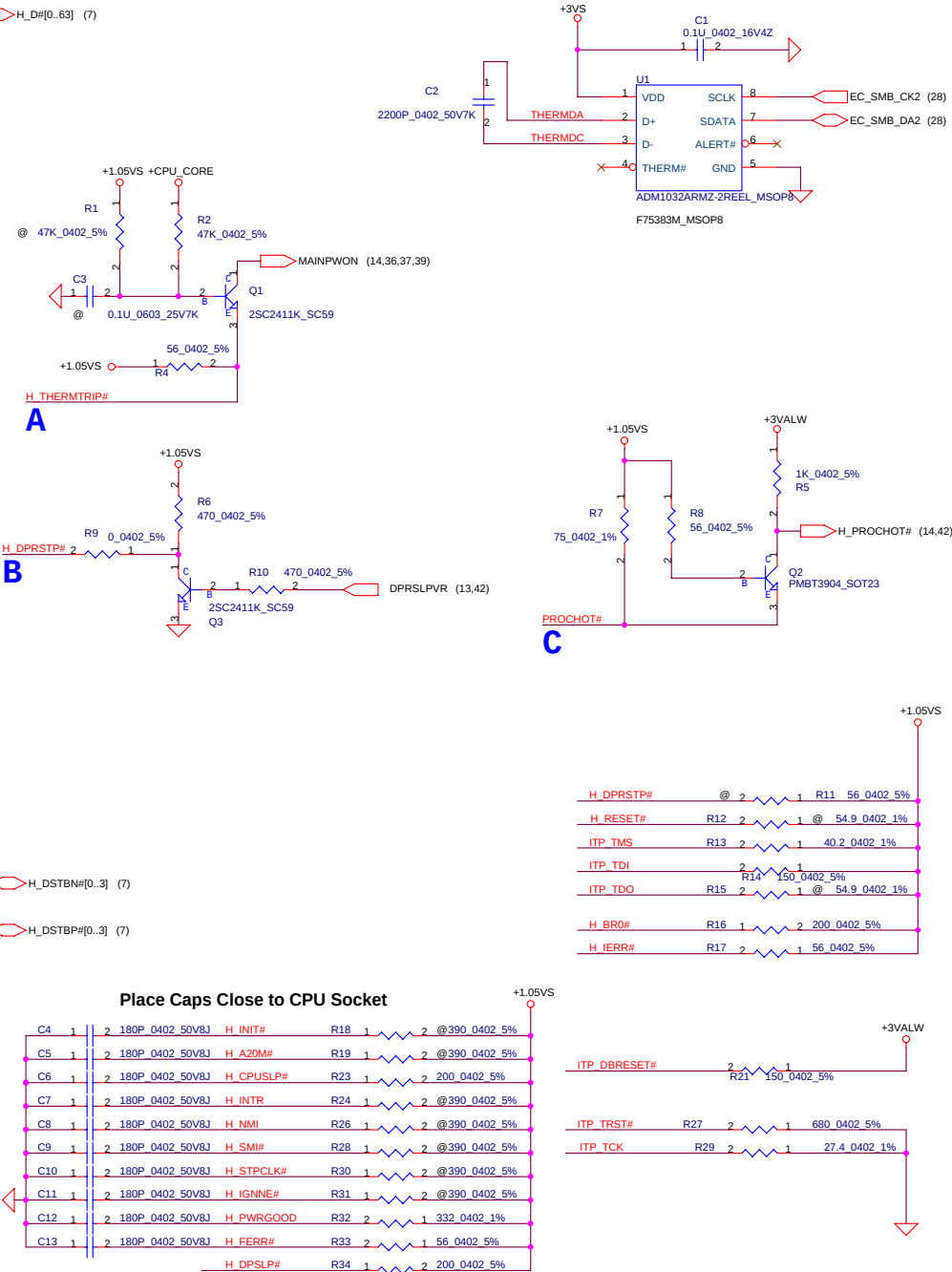
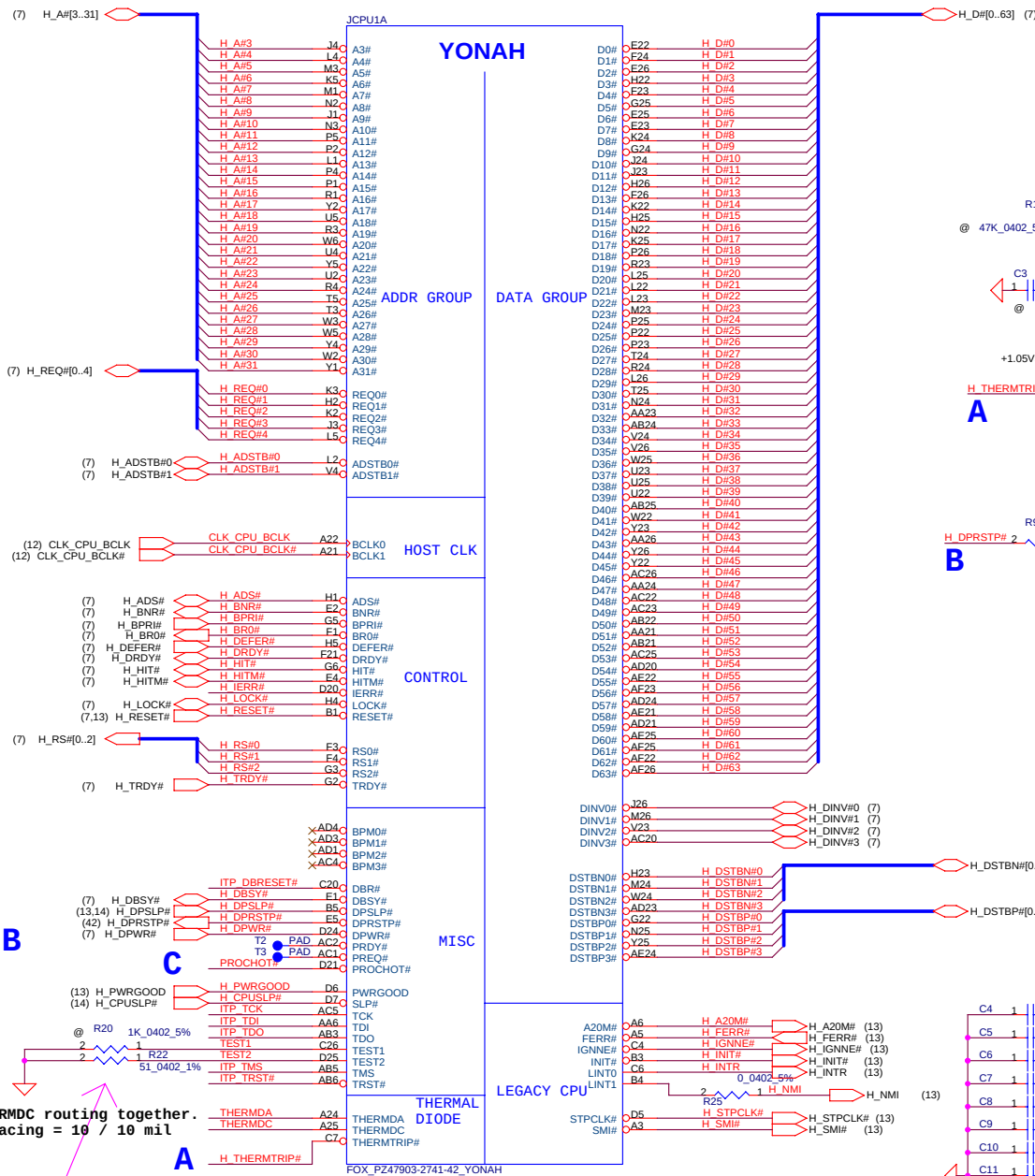
BTO Option Table

BTO Item	BOM Structure
LAN(10/100)	8100C@
LAN(GIGA)	8110S@
FIR	FIR@
MINI_CARD1	MINI1@
SATA_HDD	SATA@
CardReader	4IN1@

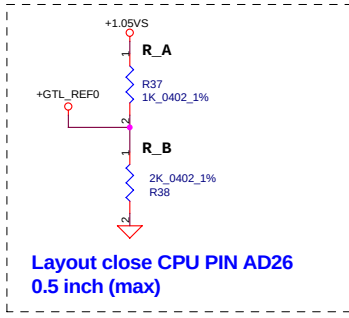
SKU ID Table

SKU ID	SKU
0	
1	
2	
3	
4	
5	
6	
7	

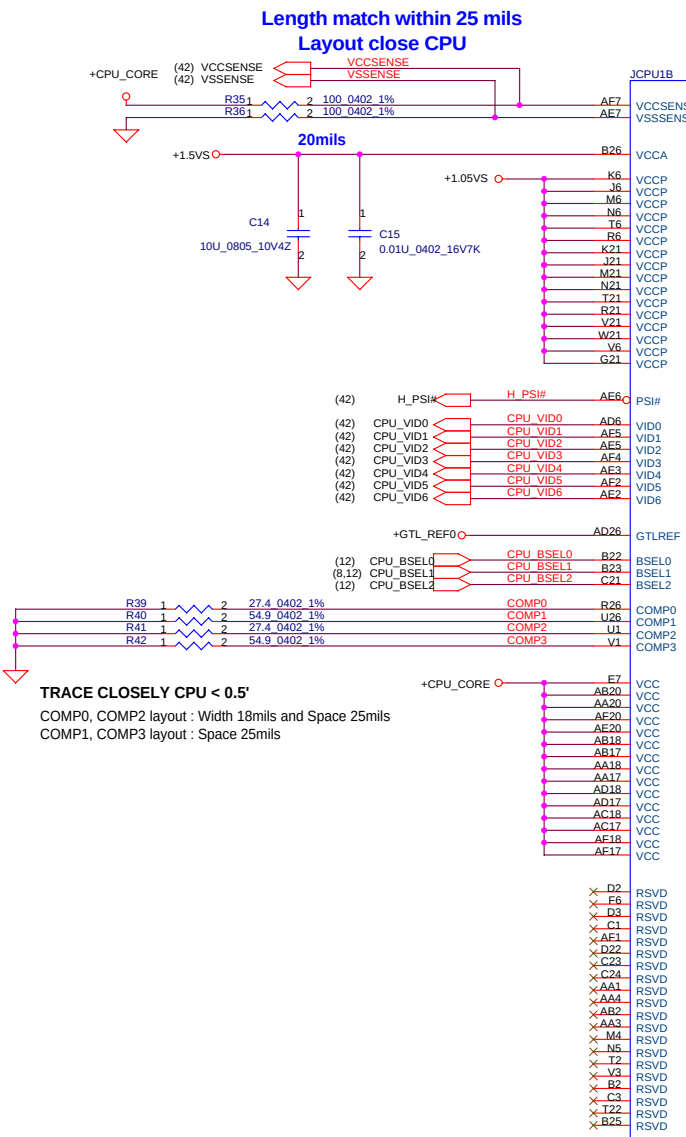
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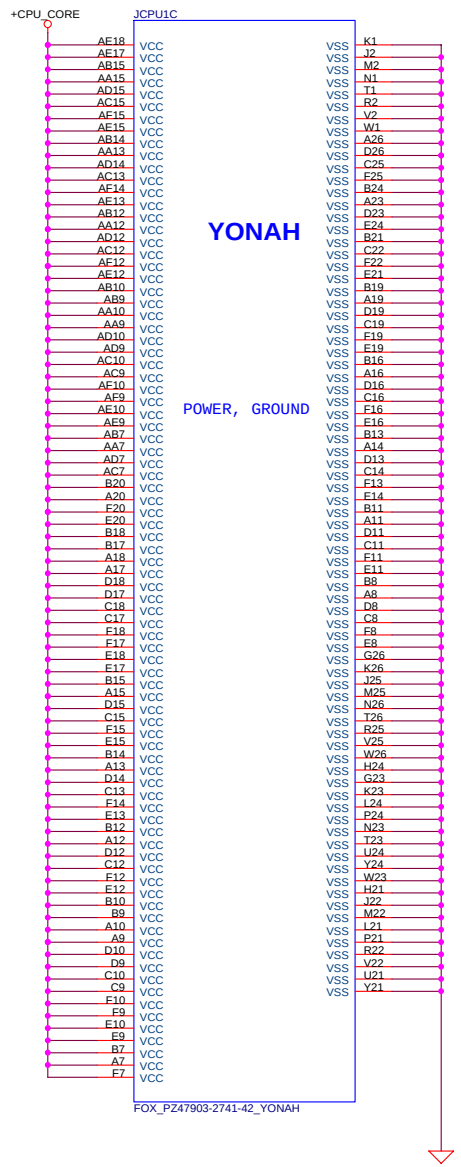
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CPU_BSEL	CPU_BSEL0	CPU_BSEL1	CPU_BSEL2
133	0	0	1
166	0	1	1

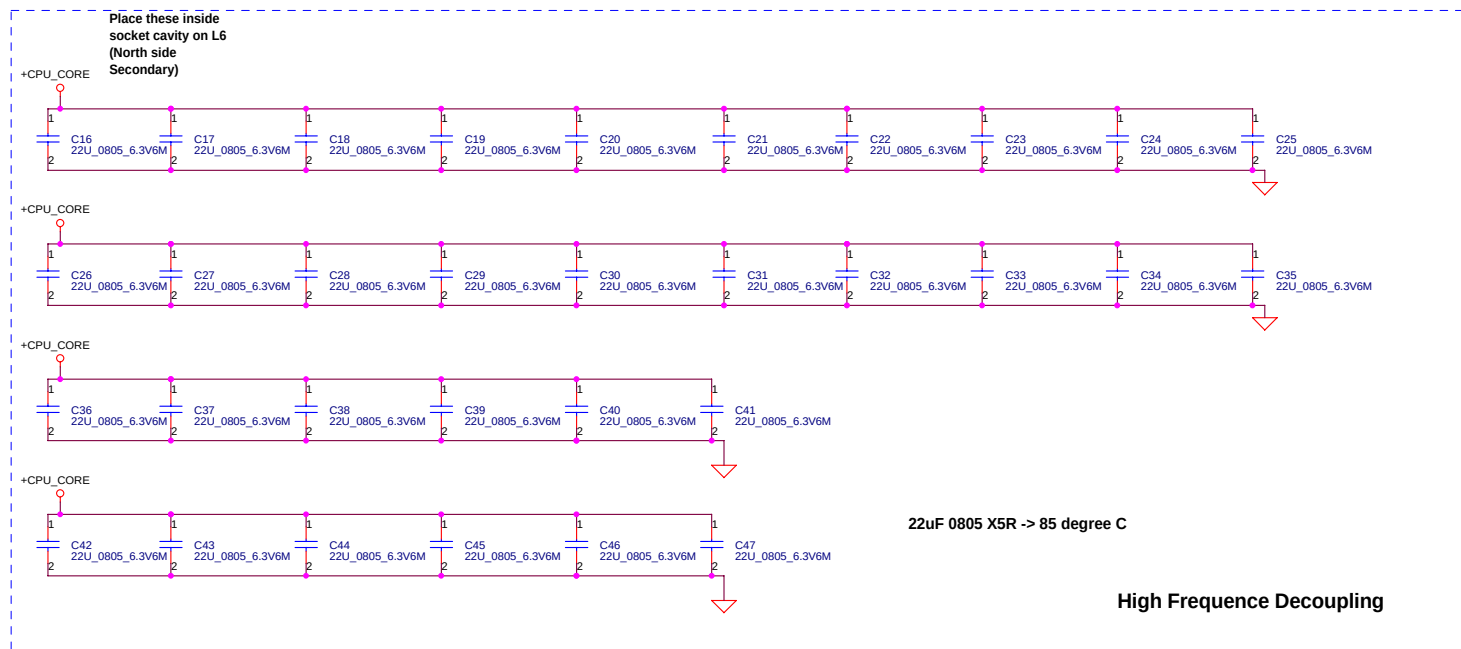


POWER, GROUND, RESERVED SIGNALS AND NC

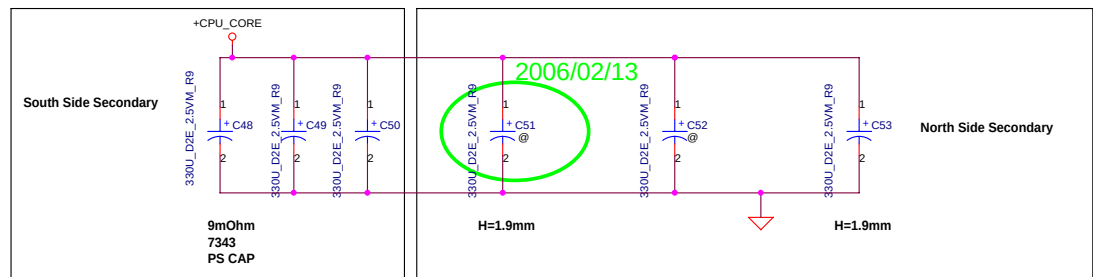


YONAH

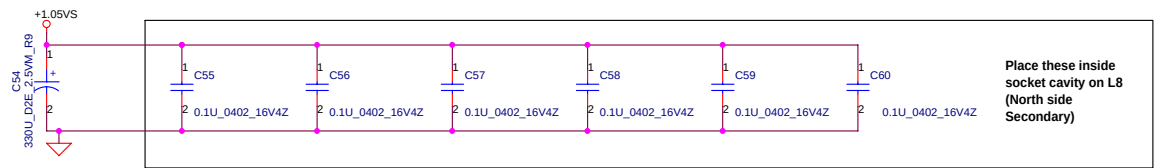
POWER, GROUND



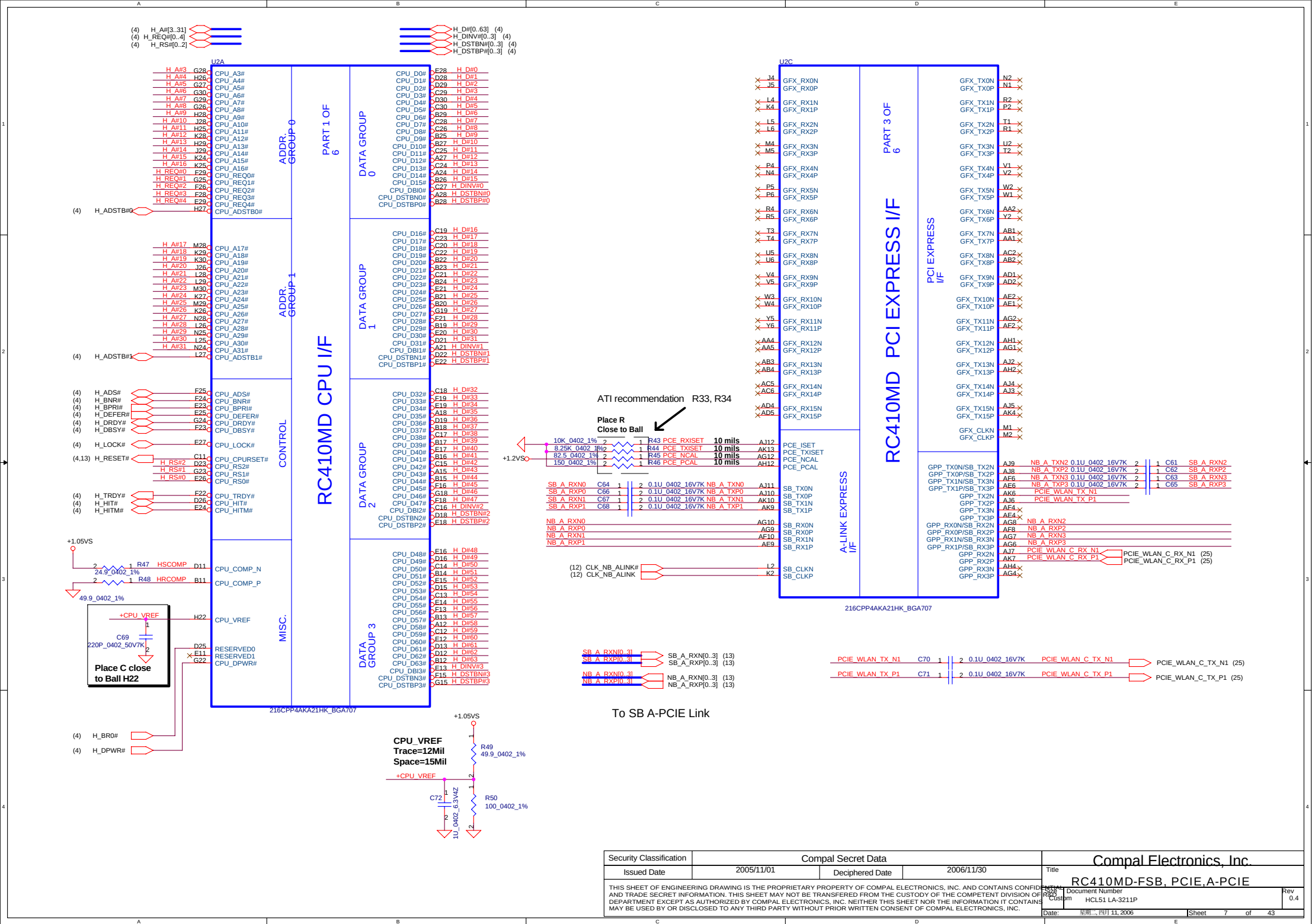
Near VCORE regulator.



ESR <= 1.5m ohm
Capacitor > 1980uF



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Layout Note:
Place near JDIM1

Layout Note:
Place one cap close to every 2 pullup
resistors terminated to V_DDR_MCH_REF

Layout Note:
Every four parallel termination resistors with two caps,
one is connected to ground, the other one is connected
between +1.8V and +0.9VS. Need to place each parallel
resistor with one cap to GND and one cap between
+1.8V and +0.9VS

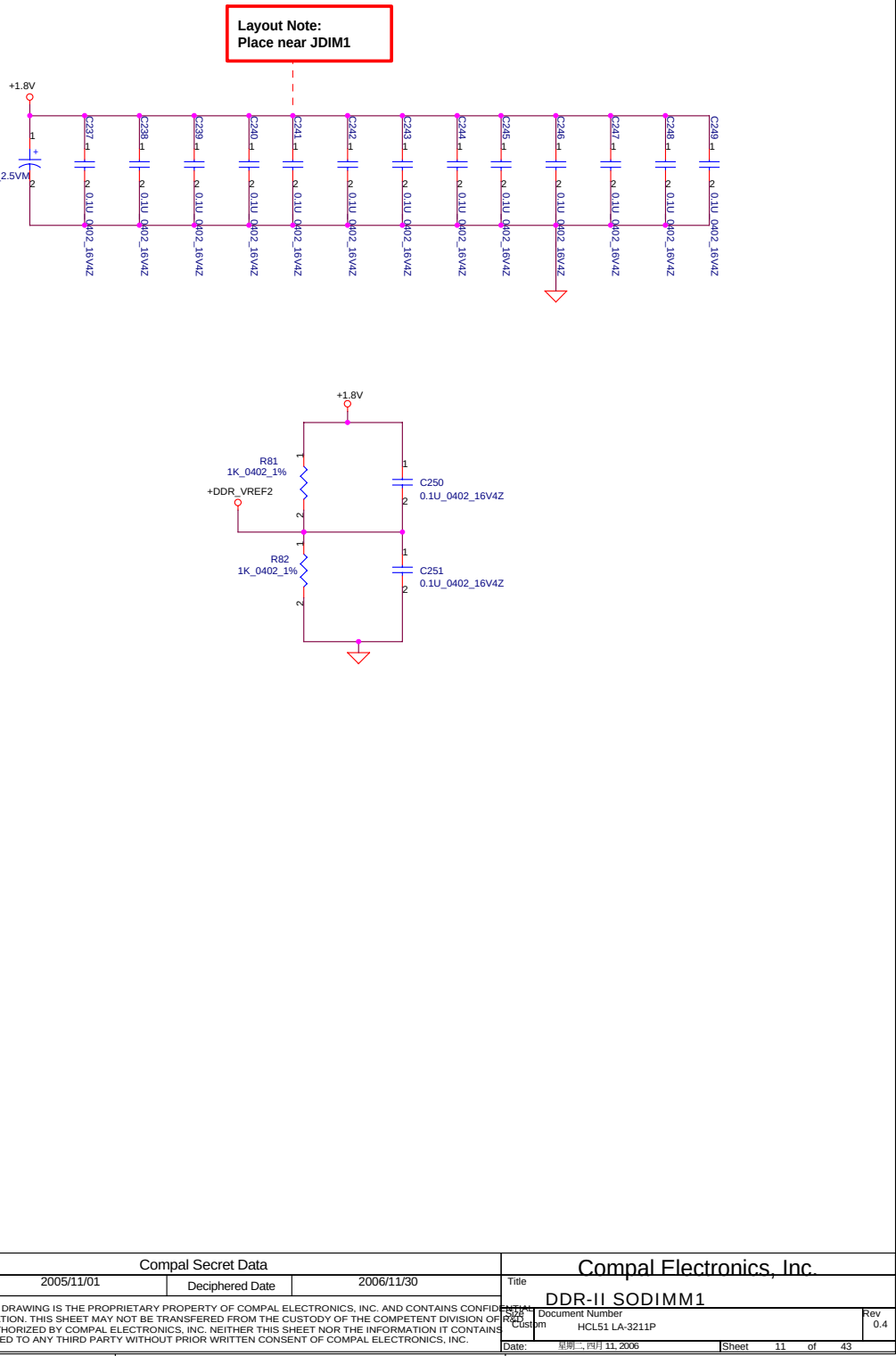
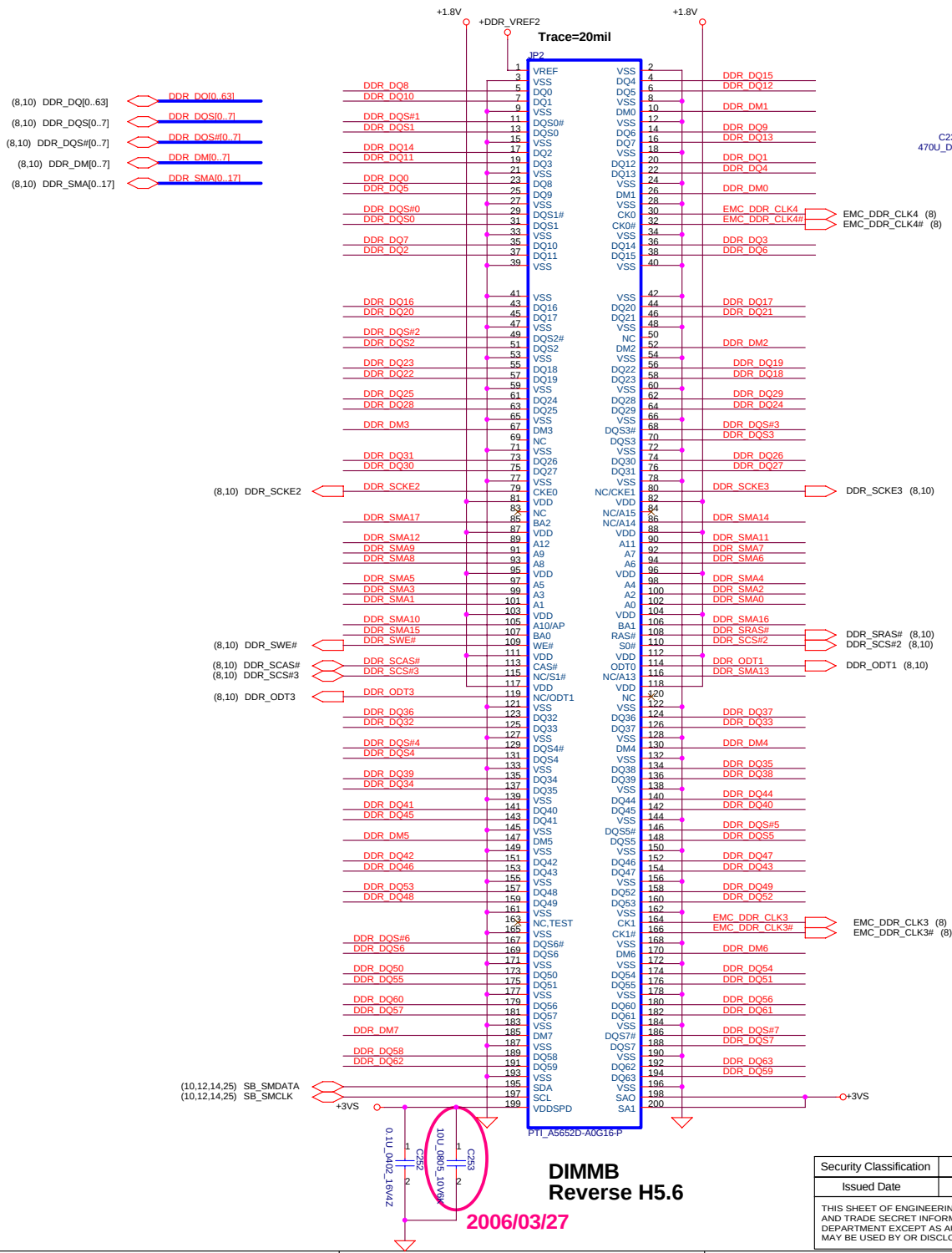
2006/01/23

2005/12/26

DIMMA
Reverse H9.2

2006/03/27

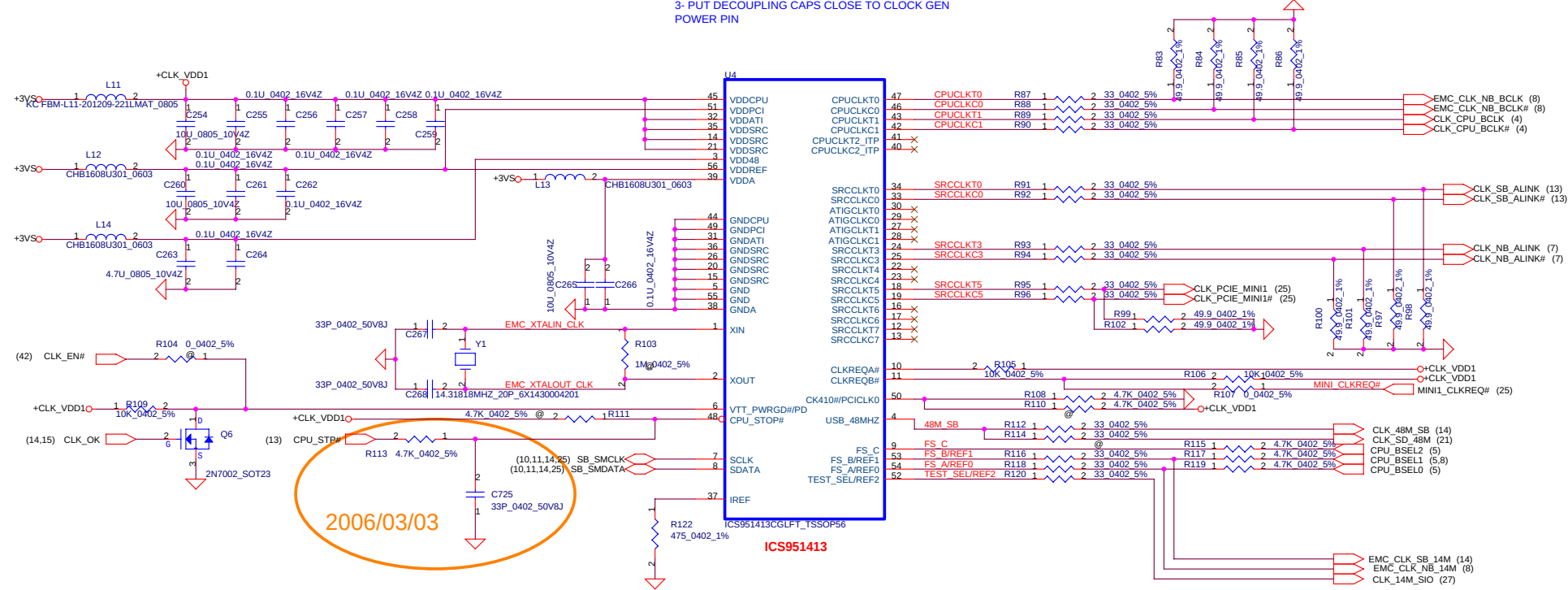
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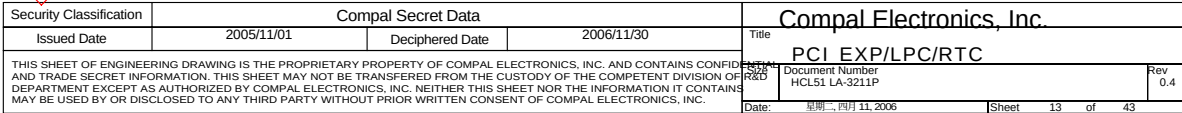
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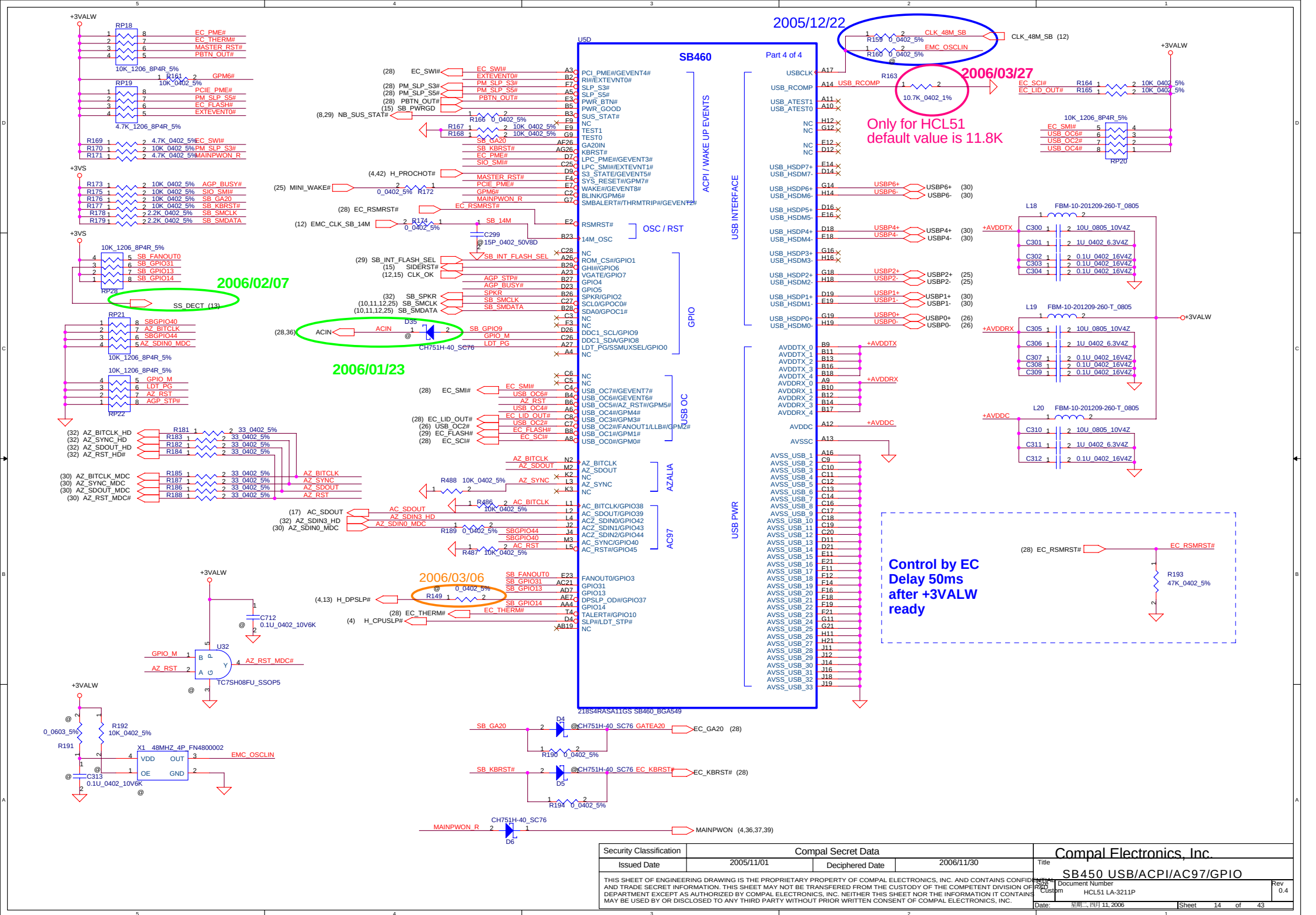
Clock Generator

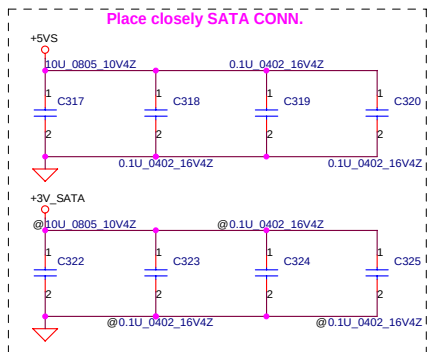
- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO CLOCK GEN AS POSSIBLE
- 2- ROUTE ALL CPUCCLK#, NBCLK#, ITPCLK# AND SRCCLK# AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO CLOCK GEN POWER PIN



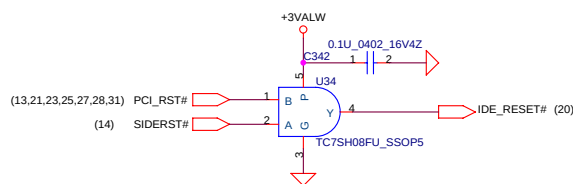
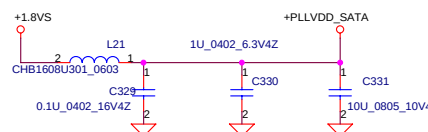
FS_C	FS_B	FS_A	CPU	SRC	PCI	REF	USB
1	0	1	100.00	100.00	33.33	14.318	48.000
0	0	1	133.33	100.00	33.33	14.318	48.000
0	1	1	166.66	100.00	33.33	14.318	48.000



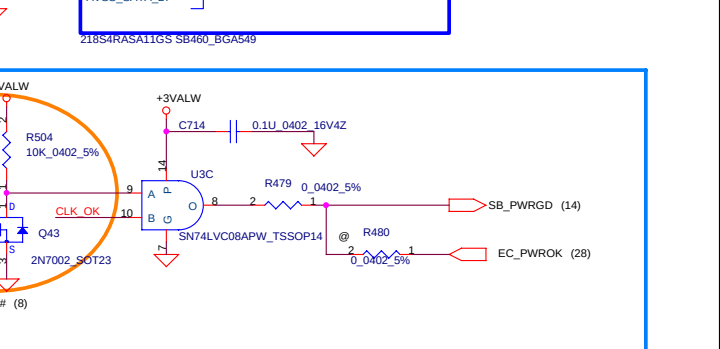
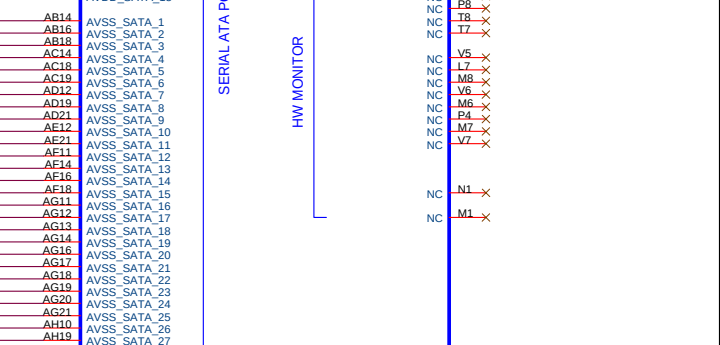
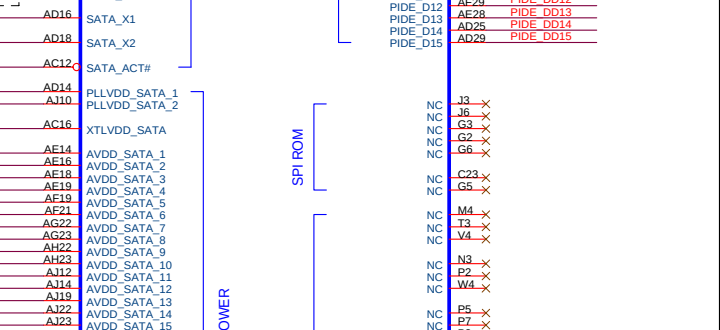
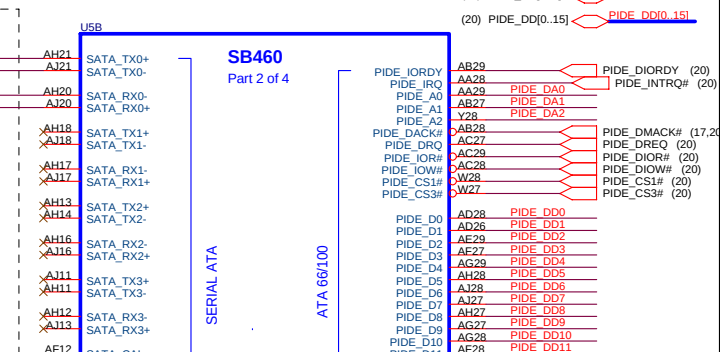
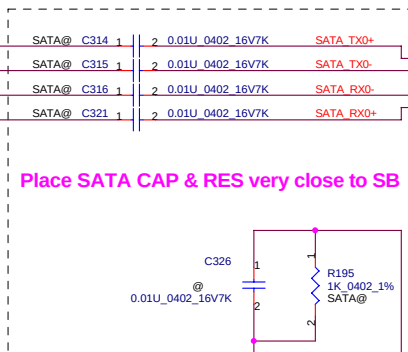
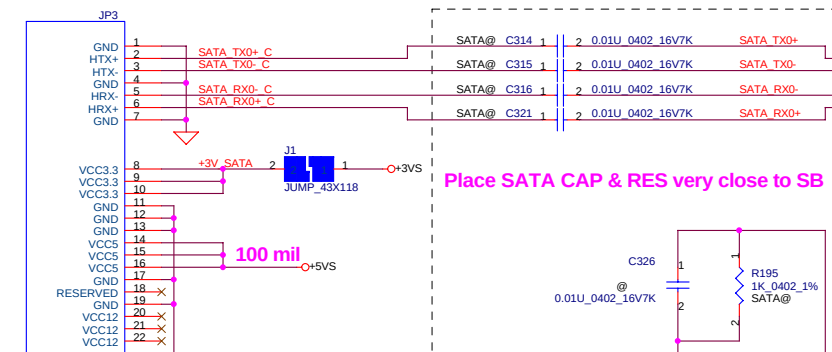
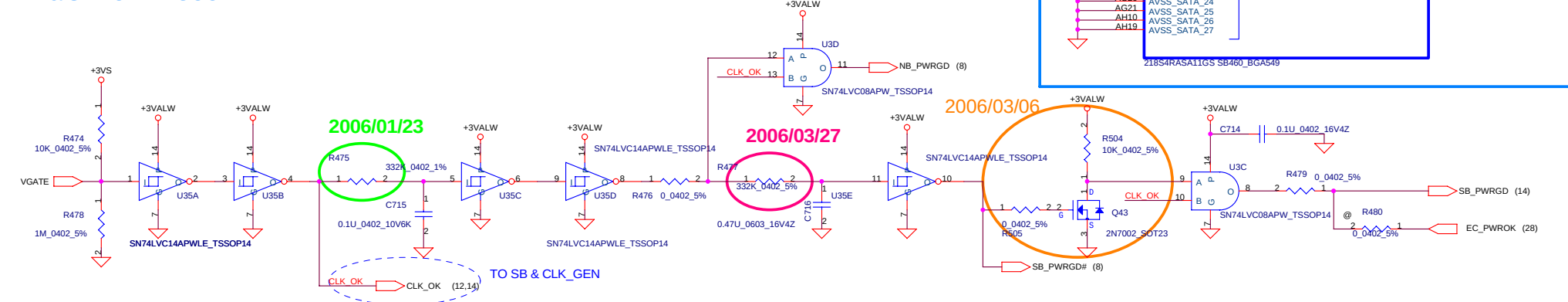




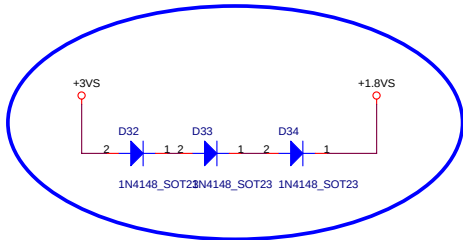
SATA HDD CONNECTOR



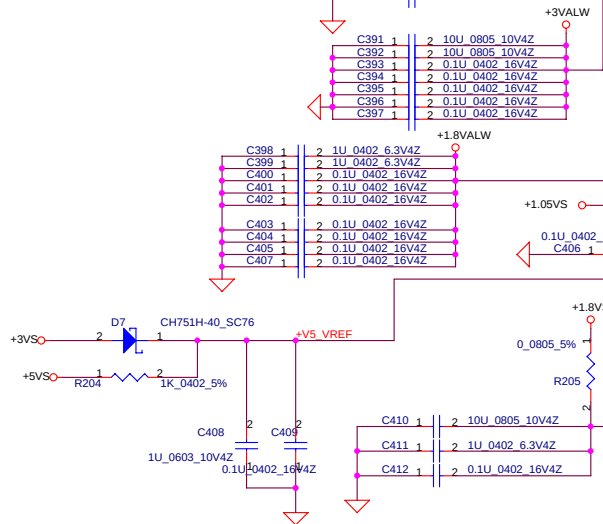
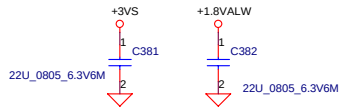
NB & SB POWER GOOD



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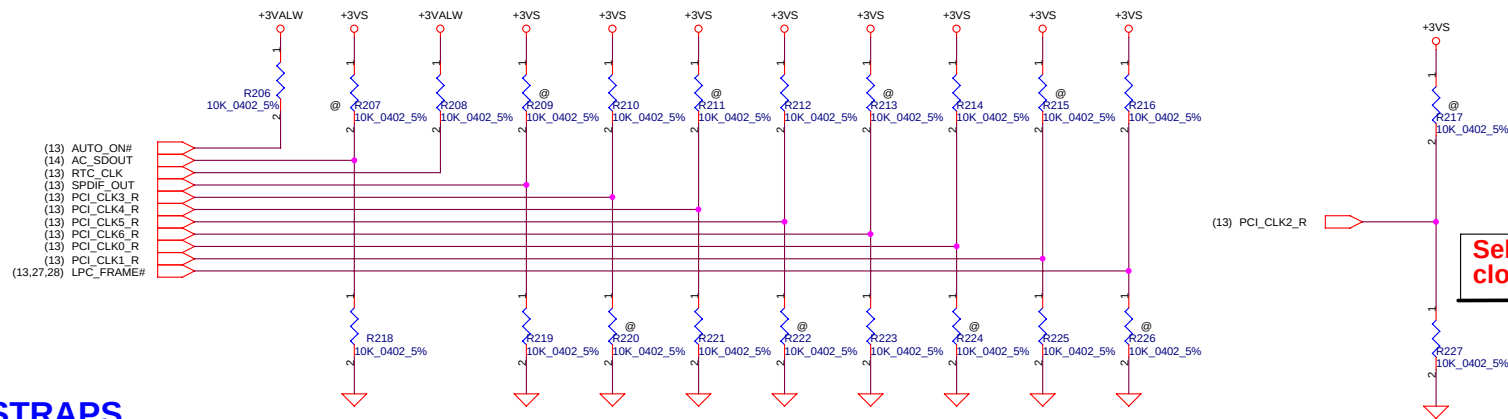


2005/12/21



+V5_VREF (20mils)
+AVDD_CK(40mils)

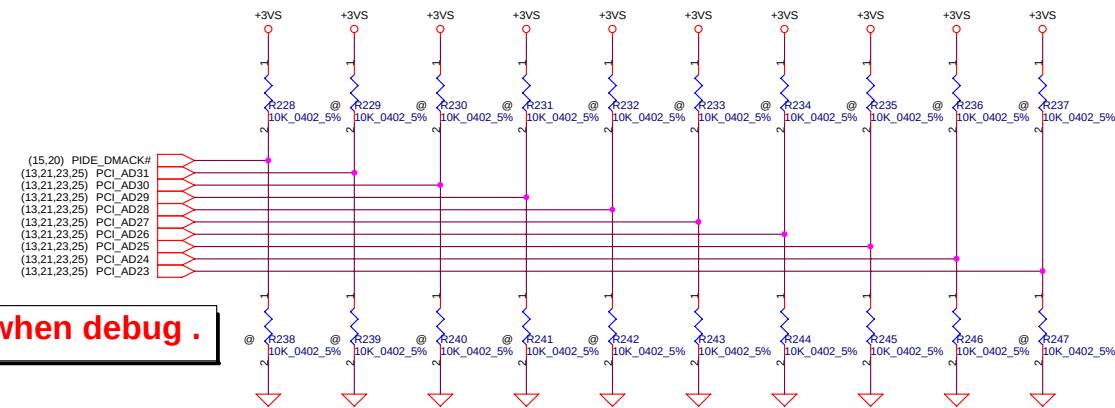
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REQUIRED STRAPS



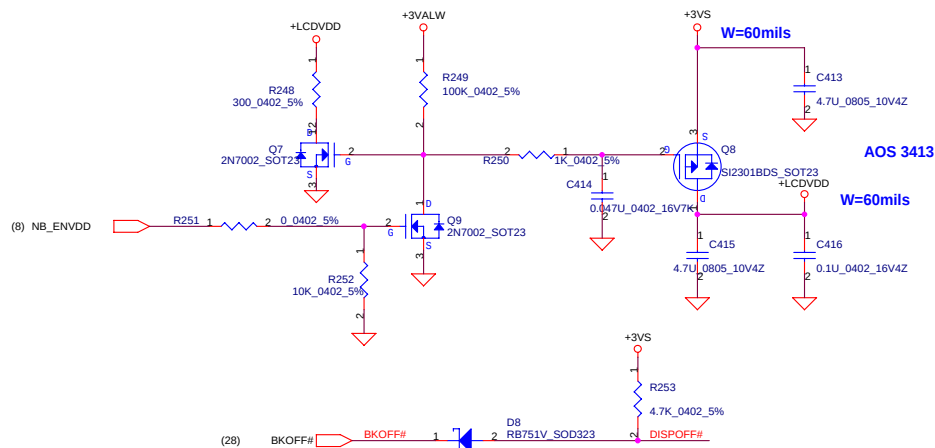
	AUTO_ON#	AC97_SDOUT	RTC_CLK	SPDIF_OUT	CLK_PCI3	CLK_PCI4	CLK_PCI5	PCI_CLK6	PCI_CLK0	PCI_CLK1	LFRAME#	CLK_PCI2
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	PU for 48Mhz XTAL mode DEFAULT	USB PHY PWRDOWN DISABLE DEFAULT	Internal PLL	PCIE AUTO detect DEFAULT	CPU I/F = K8 DEFAULT	ROM TYPE H,H = PCI ROM H,L = LPC ROM I L,H = LPC ROM II L,L = FWH ROM	THERMTRIP# ENABLE DEFAULT		Crystal Pad
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	48M OSC mode DEFAULT	USB PHY PWRDOWN ENABLE	External Clock DEFAULT	Forcing PCIE to 2 lanes (debug only)	CPU I/F = P4 DEFAULT		THERMTRIP# DISABLE		Clock input buffer DEFAULT



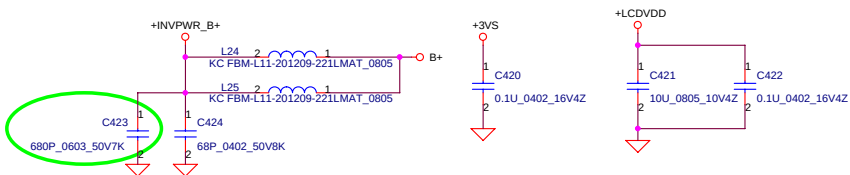
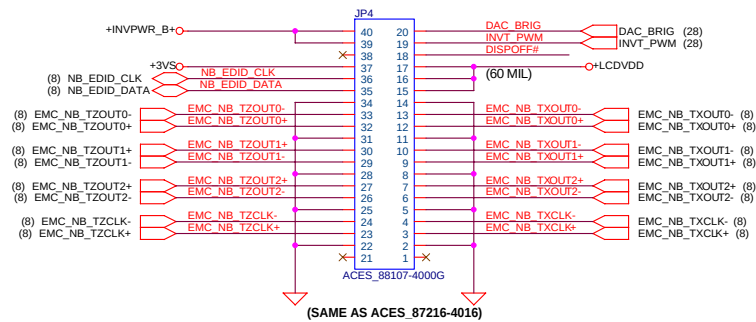
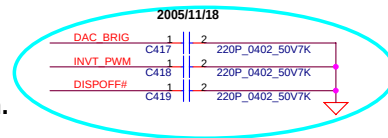
DEBUG STRAPS

	PIDE_DMACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Reserved	Reserved	Reserved	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
PULL LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS	

LCD POWER CIRCUIT

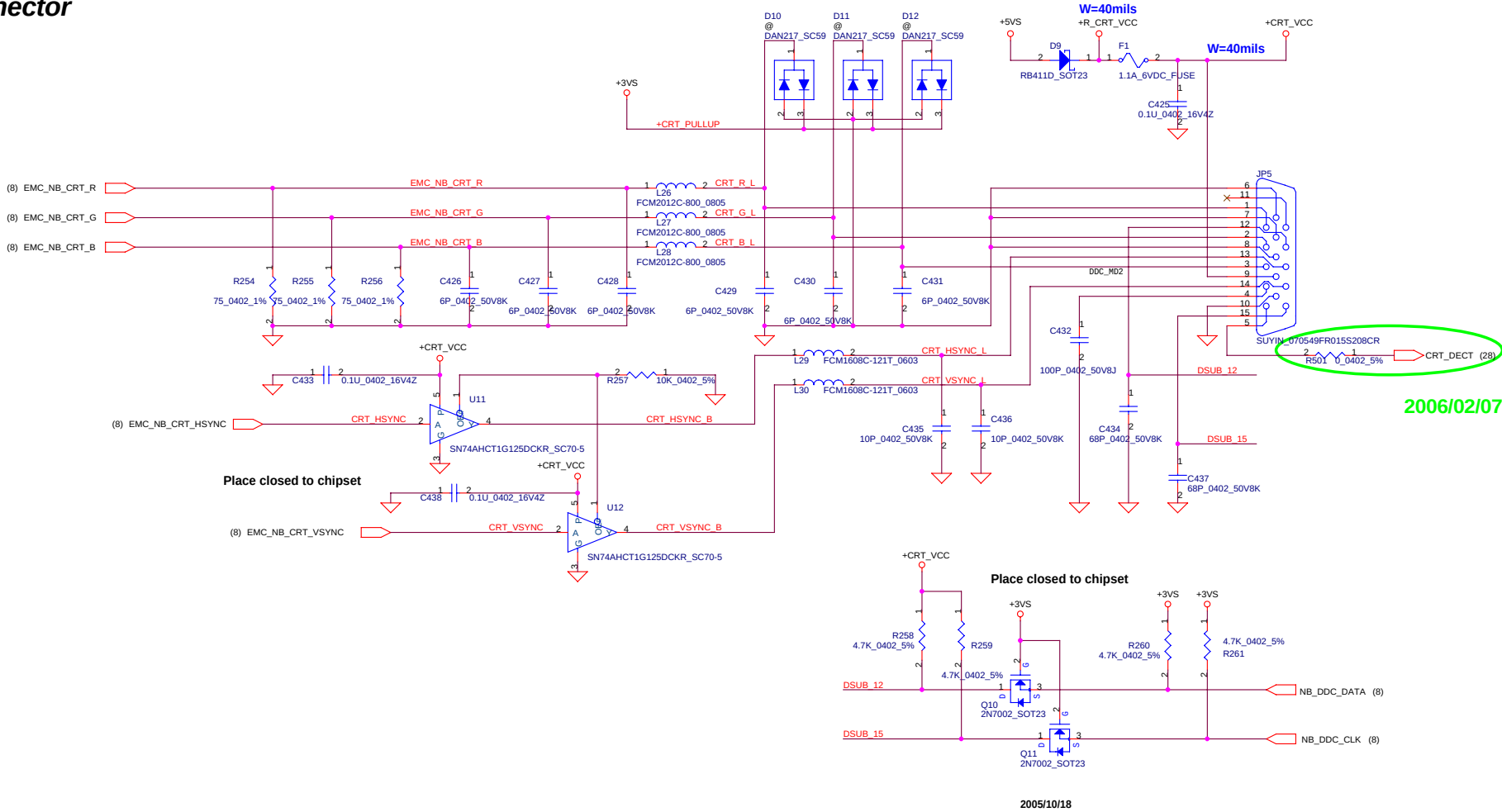


LCD/PANEL BD. Conn.

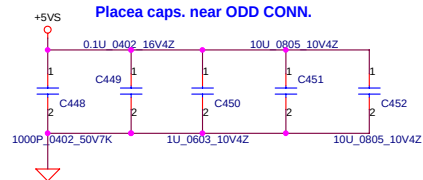


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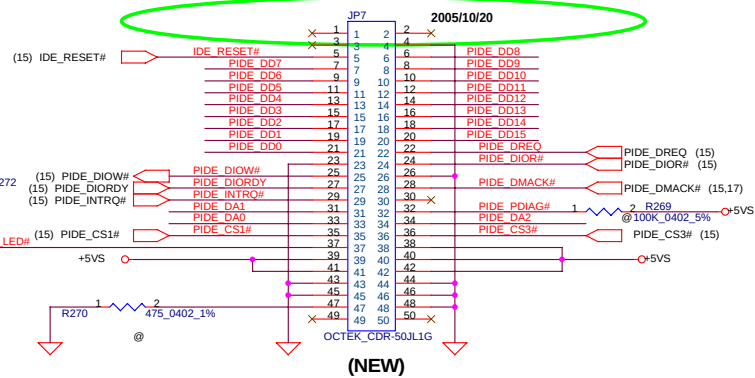
CRT Connector



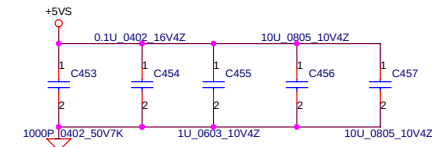
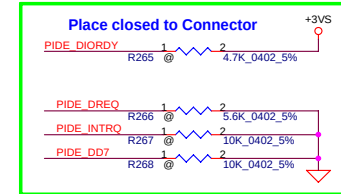
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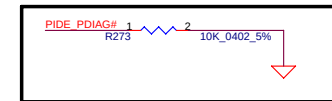
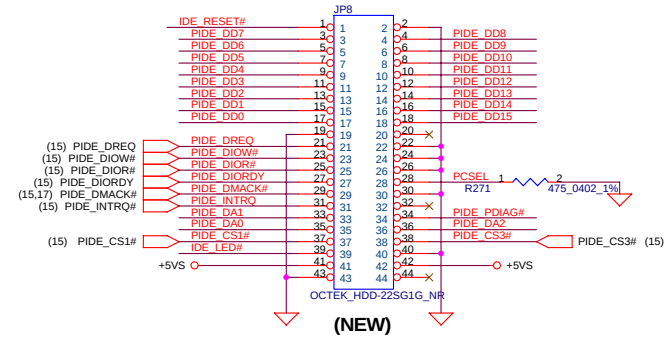
ODD Conn.



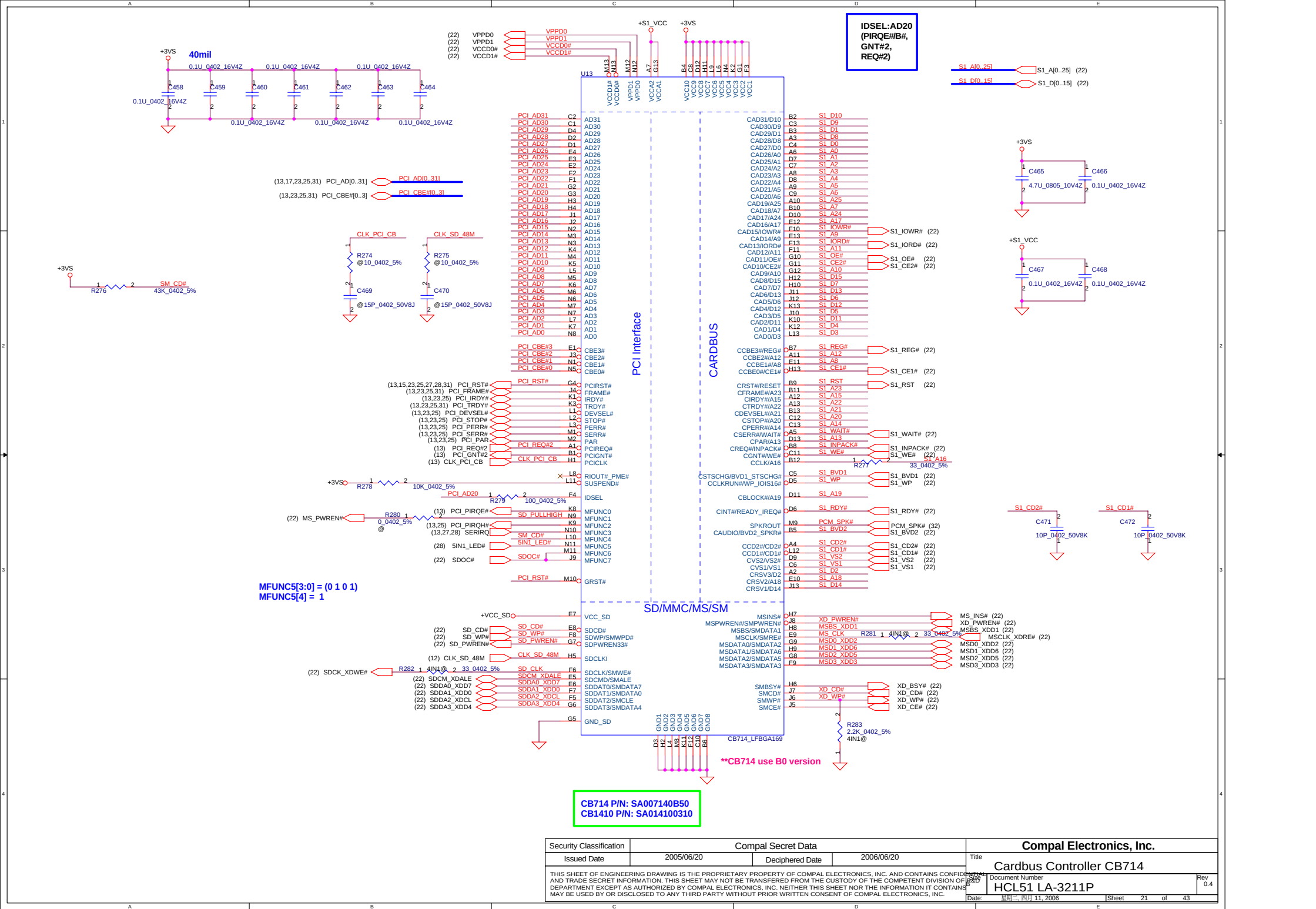
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(15) PIDE_DD[0..15] PIDE_DD[0..15]



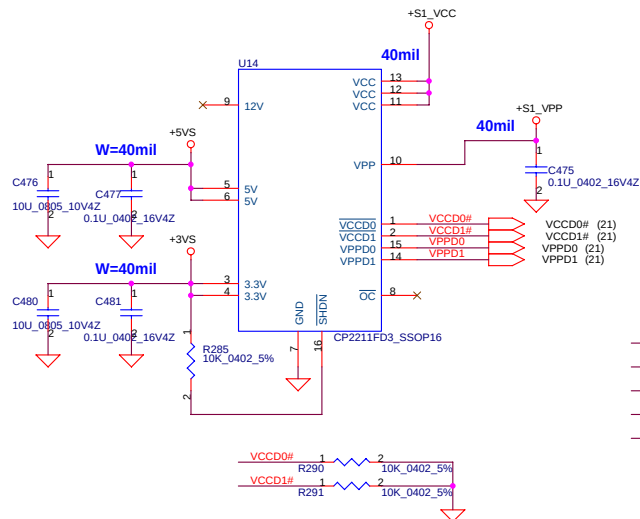
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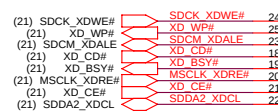
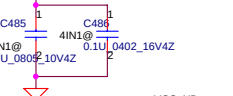
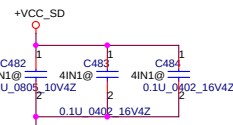
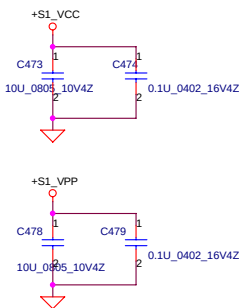
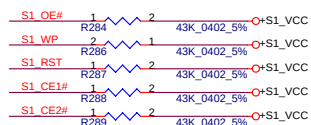
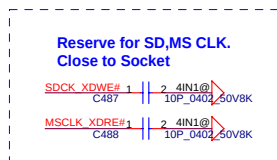
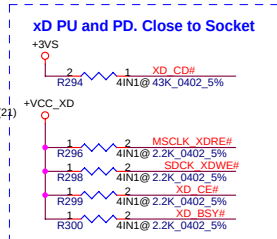
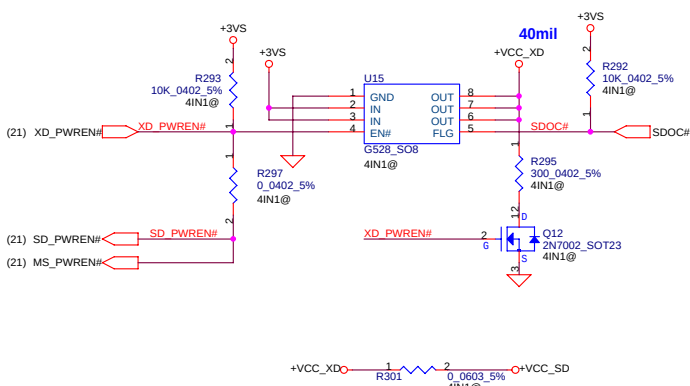
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Issued Date	2005/06/20	Deciphered Date	2006/06/20	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Title	Document Number
			ODD & SATA HDD Connector	HCL51 LA-3211P
			Date: 星期二, 四月 11, 2006	Rev 0.4
			Sheet 20	of 43



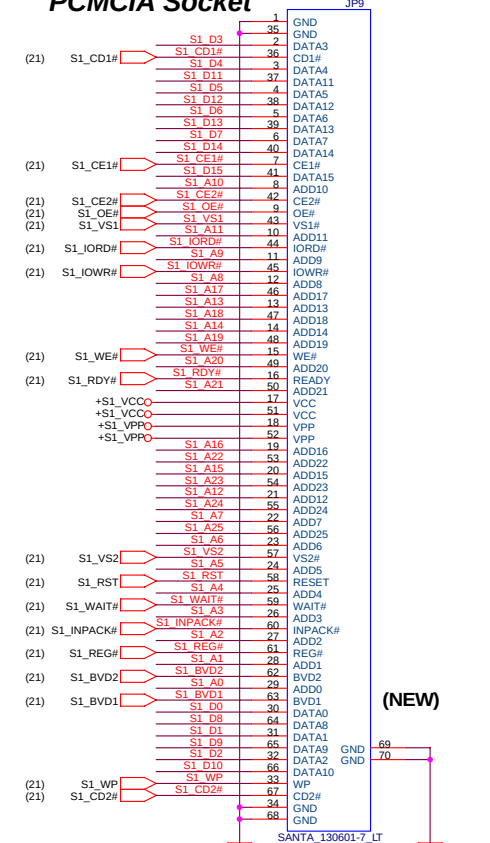
PCMCIA Power Control



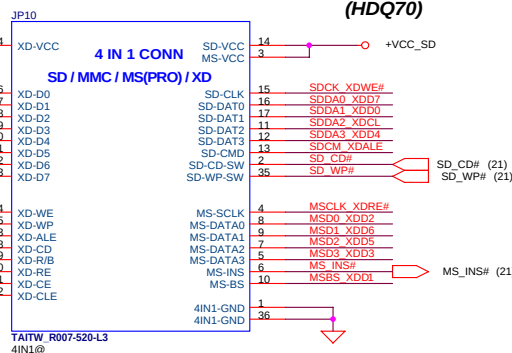
SD/MS Power Control
XD Power Control



PCMCIA Socket



4 IN 1 Socket
(HDQ70)



Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2005/06/20	Deciphered Date	2006/06/20	Title	PCMCIA Socket	
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				HCL51 LA-3211P		
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(13,17,21,25,31) PCI_AD[0..31]

PCI AD0 104
PCI AD1 103
PCI AD2 102
PCI AD3 98
PCI AD4 97
PCI AD5 96
PCI AD6 95
PCI AD7 93
PCI AD8 90
PCI AD9 89
PCI AD10 87
PCI AD11 86
PCI AD12 85
PCI AD13 83
PCI AD14 82
PCI AD15 79
PCI AD16 58
PCI AD17 57
PCI AD18 55
PCI AD19 53
PCI AD20 49
PCI AD21 47
PCI AD22 43
PCI AD23 42
PCI AD24 40
PCI AD25 37
PCI AD26 36
PCI AD27 34
PCI AD28 33
PCI AD29 32
PCI AD30 31
PCI AD31 30

IDSEL:AD22
(PIRQG#,
GNT#1,
REQ#1)

(13,21,25,31) PCI_CBE#0
(13,21,25,31) PCI_CBE#1
(13,21,25,31) PCI_CBE#2
(13,21,25,31) PCI_CBE#3

PCI AD22 46
LAN IDSEL 46

(13,21,25) PCI_PAR 76
(13,21,25,31) PCI_FRAME# 61
(13,21,25) PCI_IRDY# 63
(13,21,25,31) PCI_TRDY# 67
(13,21,25) PCI_DEVSEL# 68
(13,21,25) PCI_STOP# 69

(13,21,25) PCI_PERR# 70
(13,21,25) PCI_SERR# 75

(13) PCI_REQ#1 30
(13) PCI_GNT#1 29

(13) PCI_PIRQG# 25
(25,28) LAN_PME# 31

(13,15,21,25,27,28,31) PCI_RST# 27
RST# 27

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(13,25,27) PM_CLKRUN# 65

CLK PCI LAN 28
PM_CLKRUN# 65

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(13,25,27) PM_CLKRUN# 65

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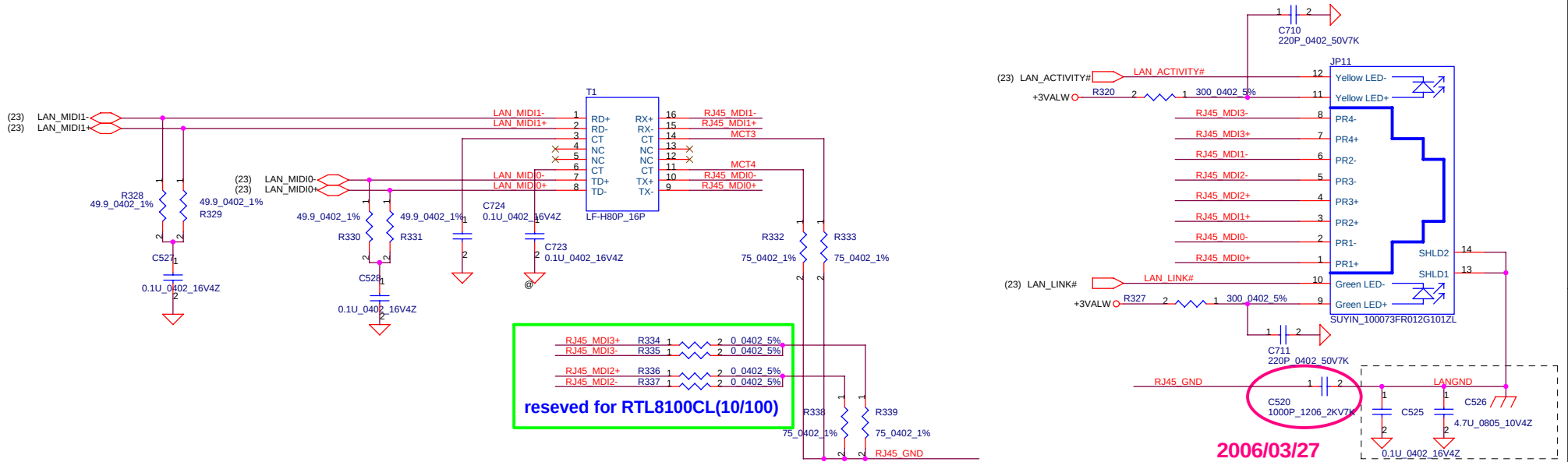
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EEDO 108
AUX/EEDO 109
EESK 102
EECS 106
LED0 117
LED1 115
LED2 114
NC/LED3 113
TXD+/MDIO+ 1
TXD-/MDIO- 2
RXIN+/MDI1+ 5
RXIN-/MDI1- 6
NC/MDI2+ 14
NC/MDI2- 15
NC/MDI3+ 18
NC/MDI3- 19
X1 121
X2 122
AD22 105
LWAKE 23
ISOLATE# 127
RTSET 72
NC/SMBCLK 74
NC/SMBDATA 88
NC/M66EN 10
NC/AVDDH 120
AVDDH 11
NC/HSDAC+ 123
NC/HG 124
NC/VSS 9
NC/VSS 13
NC/GND 22
NC/GND 48
NC/GND 62
NC/GND 73
NC/GND 112
NC/GND 118
CTRL25 8
CTRL12 125
VDD33 26
VDD33 41
VDD33 56
VDD33 71
VDD33 84
VDD33 94
VDD33 107
AVDDL 3
AVDDL 7
AVDDL 20
AVDDL 16
VDD12 126
VDD12 32
VDD12 54
VDD12 78
VDD12 99
NC/VDD12 24
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NC/VDD12 116
NC 12
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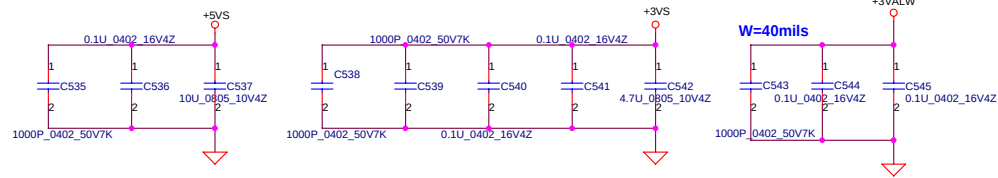
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LINK_100# 115
LINK_1000# 114
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LAN MDIO- (24) 2
LAN MDI1+ (24) 5
LAN MDI1- (24) 6
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LAN X2 122
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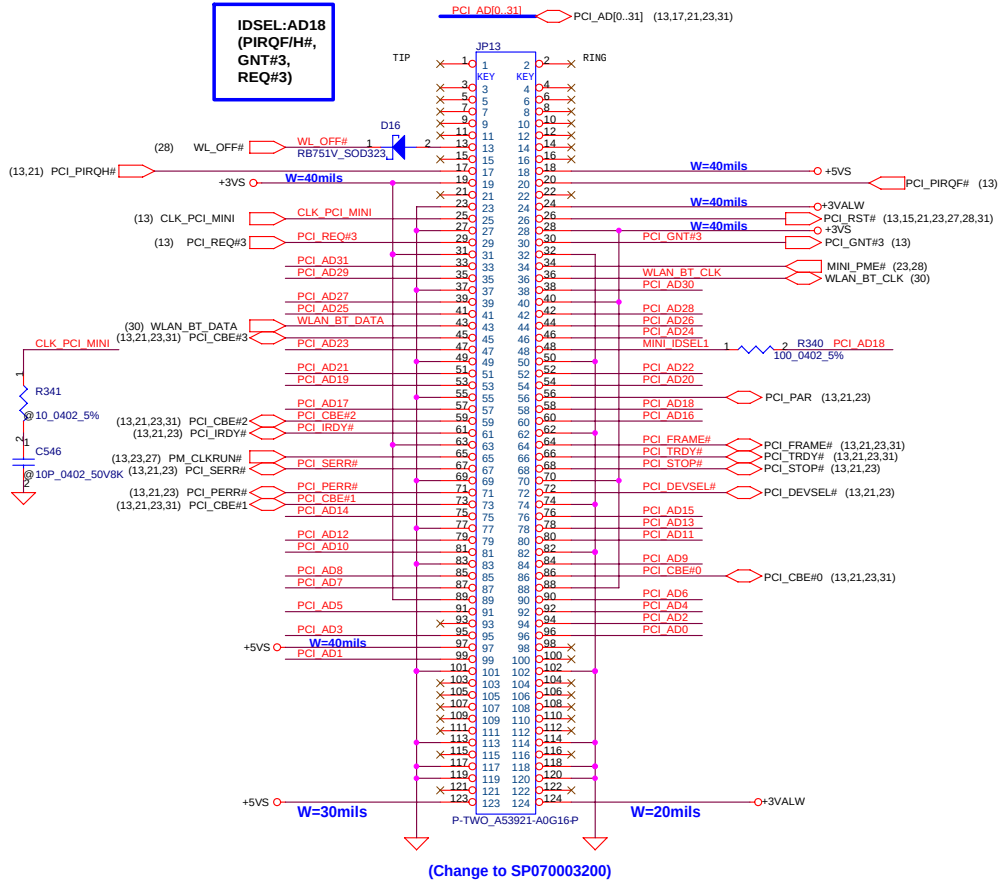
LAN RTL8100CL



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				HCL51 LA-3211P	0.4
Date: 星期二, 四月 11, 2006				Sheet	24 of 43

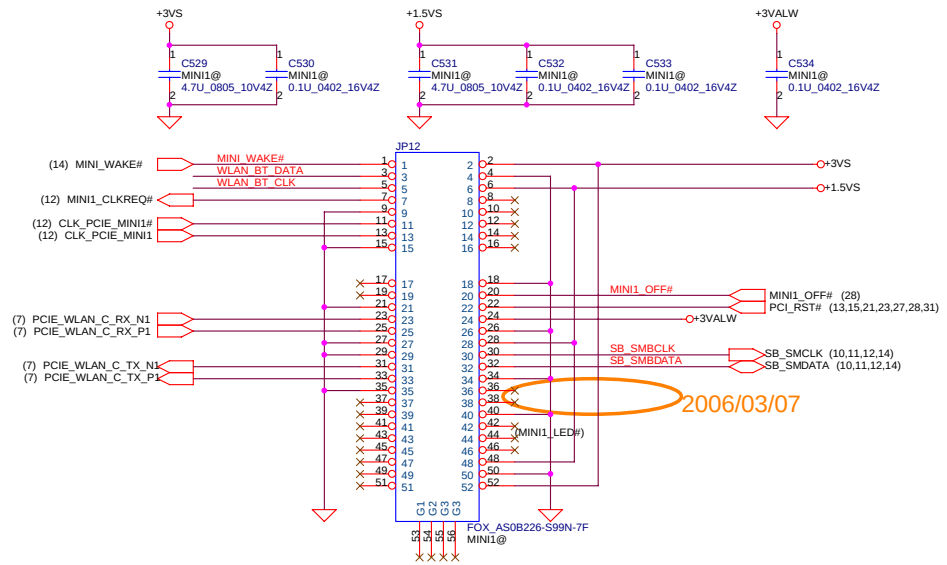


**IDSEL:AD18
(PIRQ#IH#,
GNT#3,
REQ#3)**



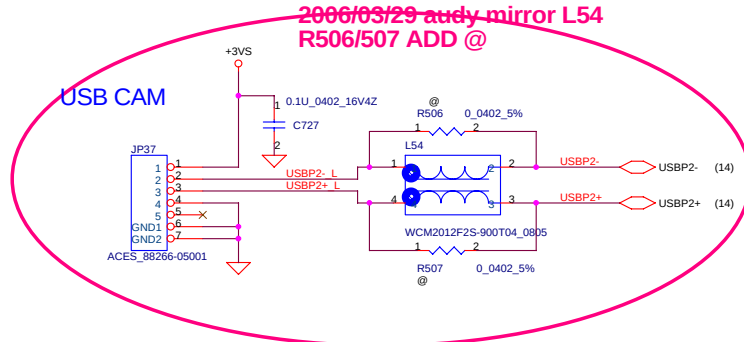
(Change to SP070003200)

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



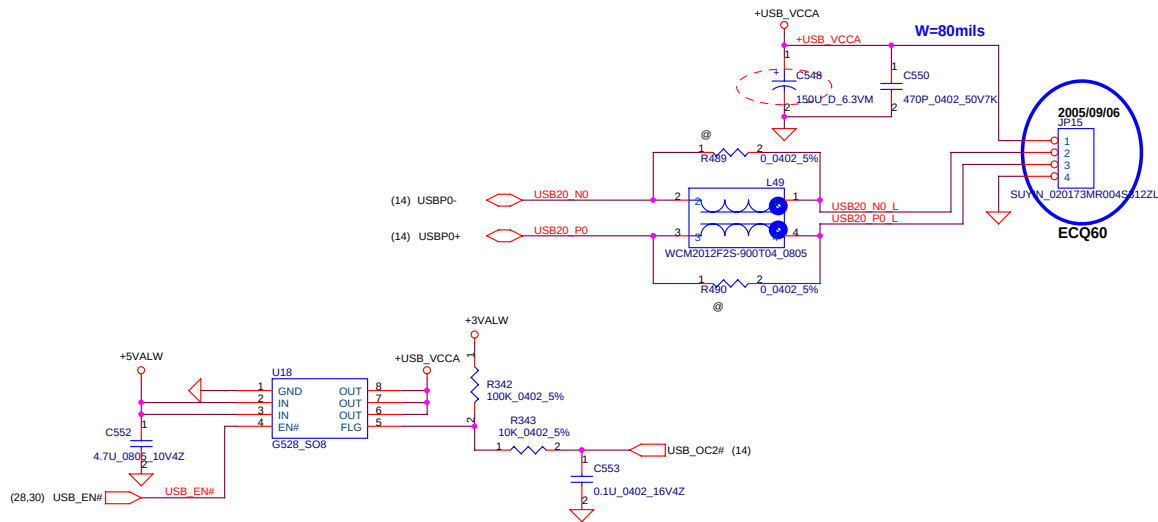
2006/03/07

2006/03/29 add mirror L54
R506/507 ADD @



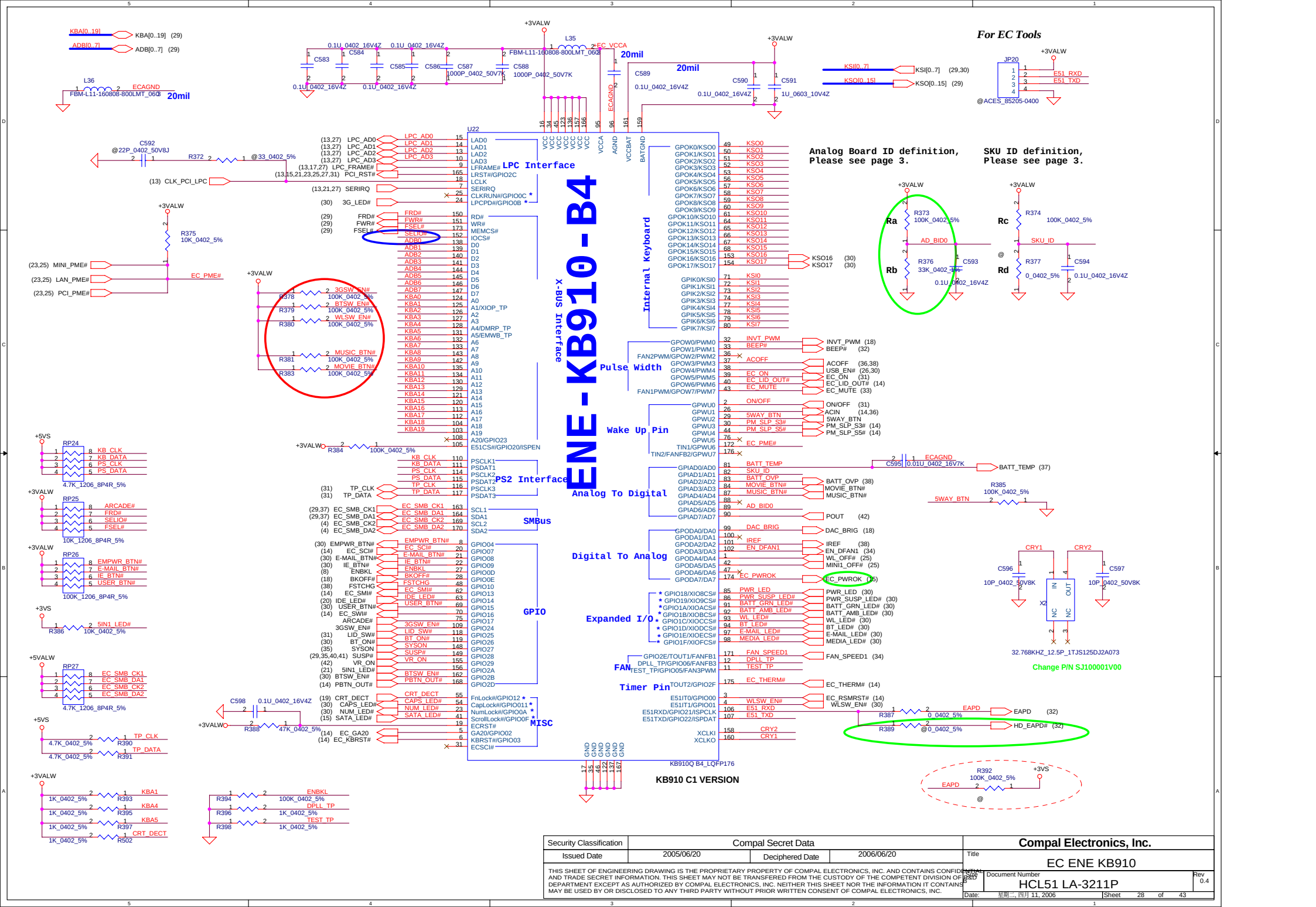
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Document Number				HCL51 LA-3211P	
Date: 星期二, 四月 11, 2006				Rev 0.4	
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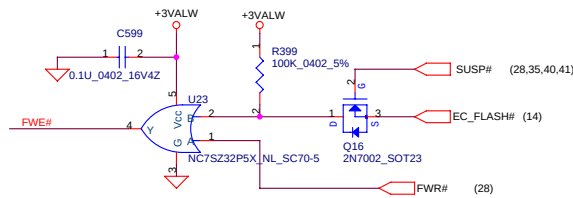
USB CONN. 1 & 2



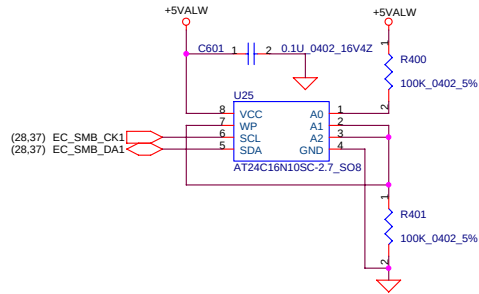
1207 DEL

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				Date	星期二, 四月 11, 2006
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				Rev	0.4

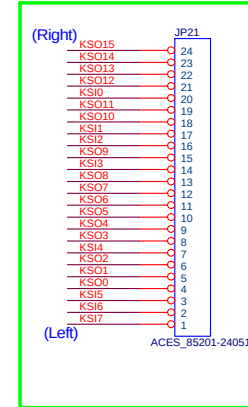
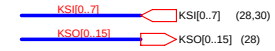




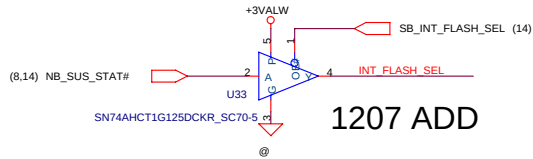
Check PCB Footprint



INT_KBD Conn.

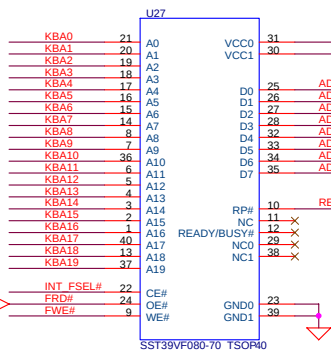


FOR DEBUG ONLY

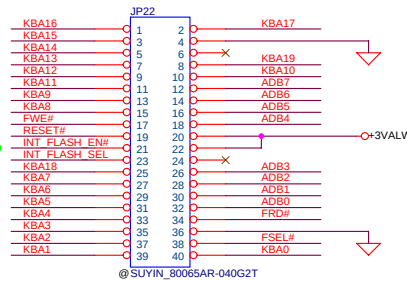


1MB Flash ROM

(28) KBA[0..19] ADB[0..7]

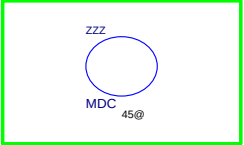


1MB ROM Socket

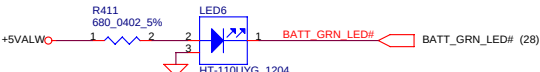
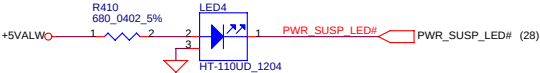
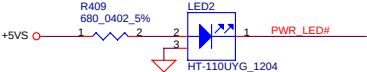
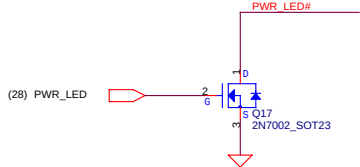
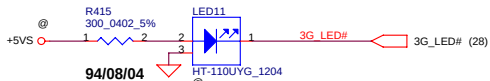
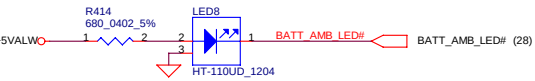


2006/01/23
DEL SB_INT_FLASH_SEL

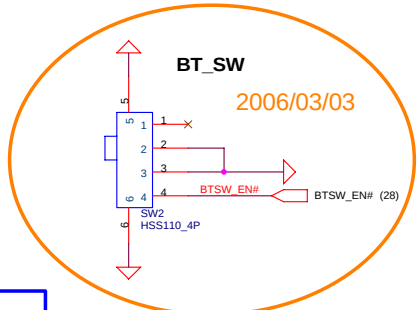
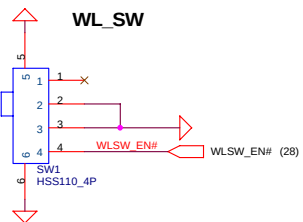
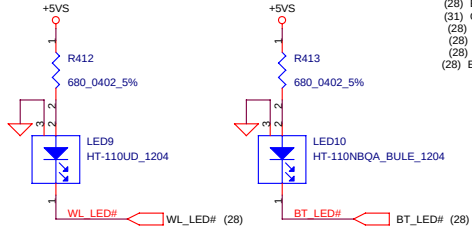
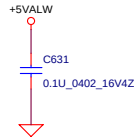
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				Date	2006/04/11
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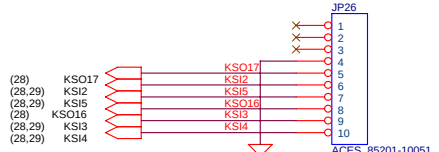
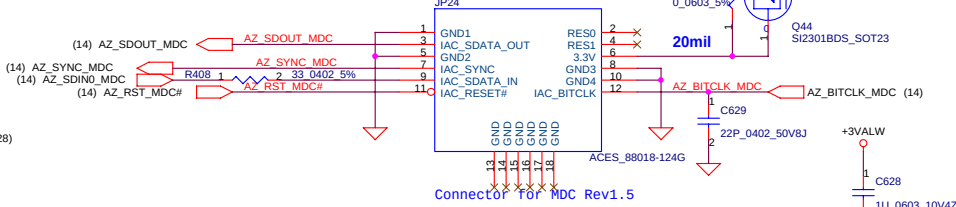
2006/01/23



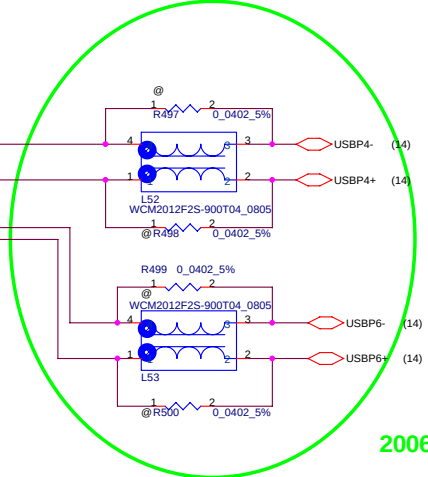
To LED/B Conn.



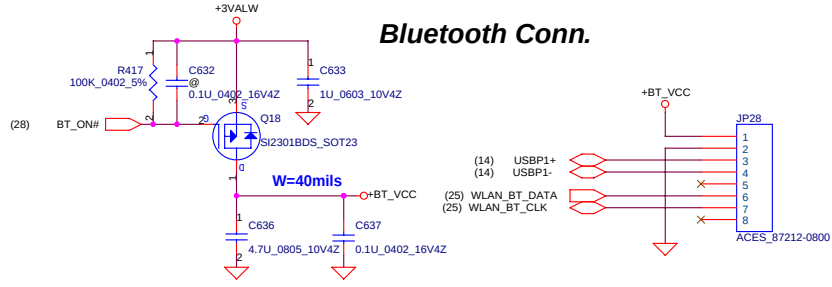
MDC Conn.



2006/01/24

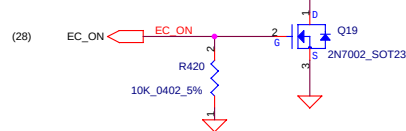
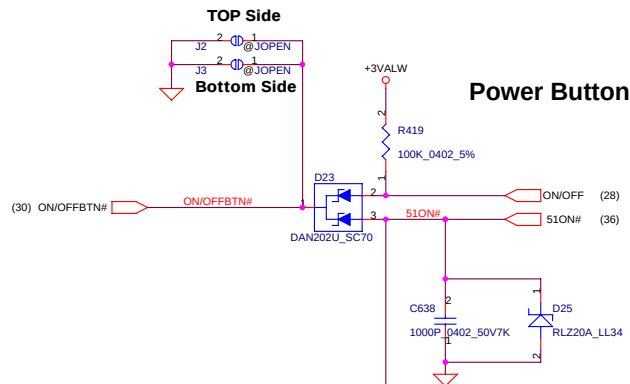


Bluetooth Conn.

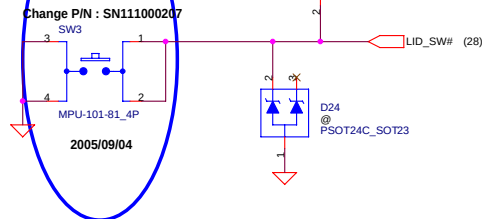


Geneva			Grapevine		
	KSO16	KSO17		KSO16	KSO17
KSI0	VOL_UP	LEFT			
KSI1	RIGHT	VOL_DOWN			
KSI2	PLAY	ENTER			
KSI3	STOP				
KSI4	NEXT				
KSI5	REV				
KSI6		RECORD			

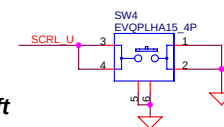
ON/OFF switch



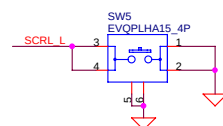
Lid Switch



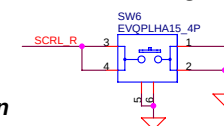
Scroll Up



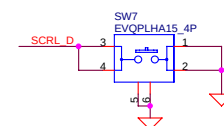
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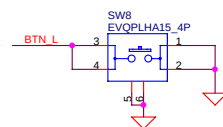
Scroll Right



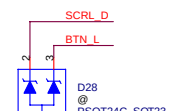
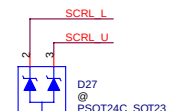
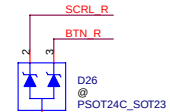
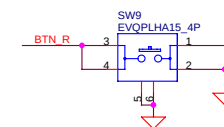
Scroll Down



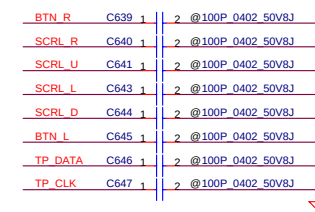
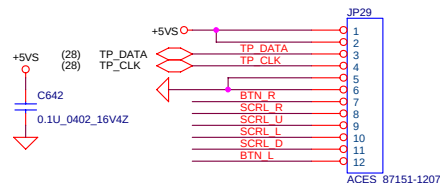
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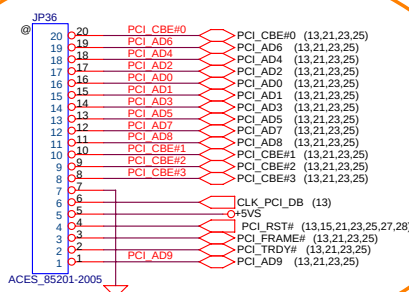
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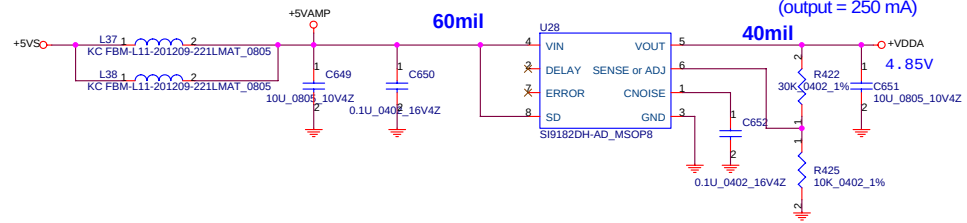
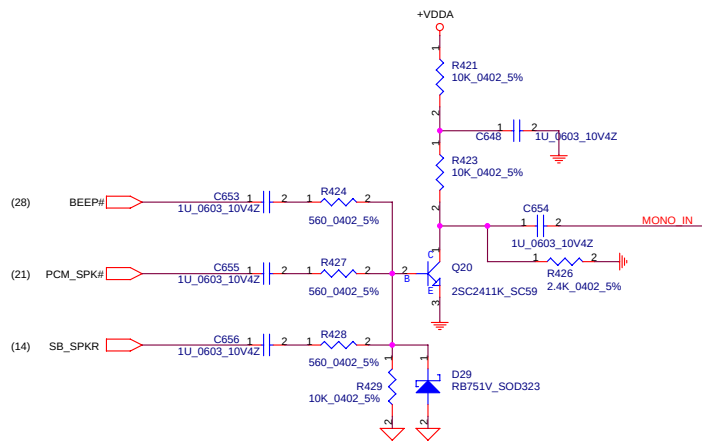
To TP/B Conn.



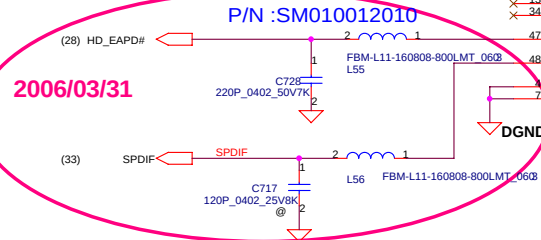
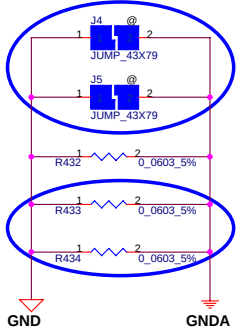
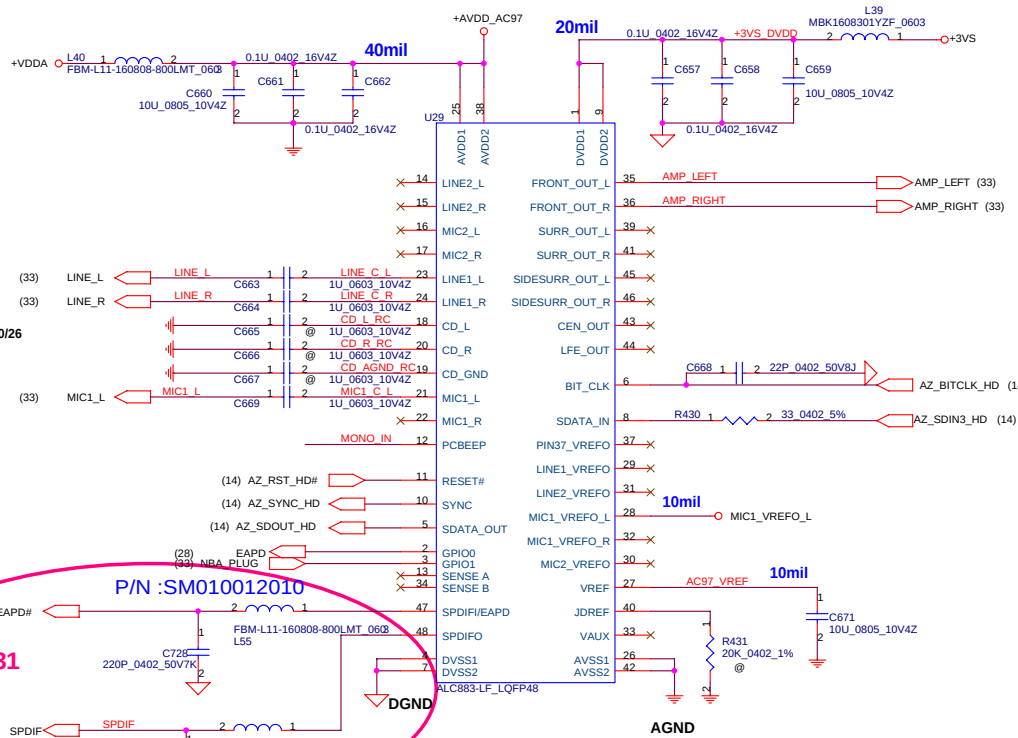
2006/03/07



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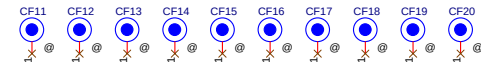
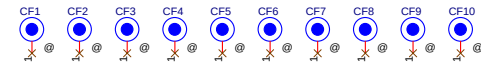
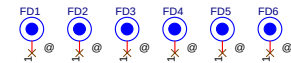
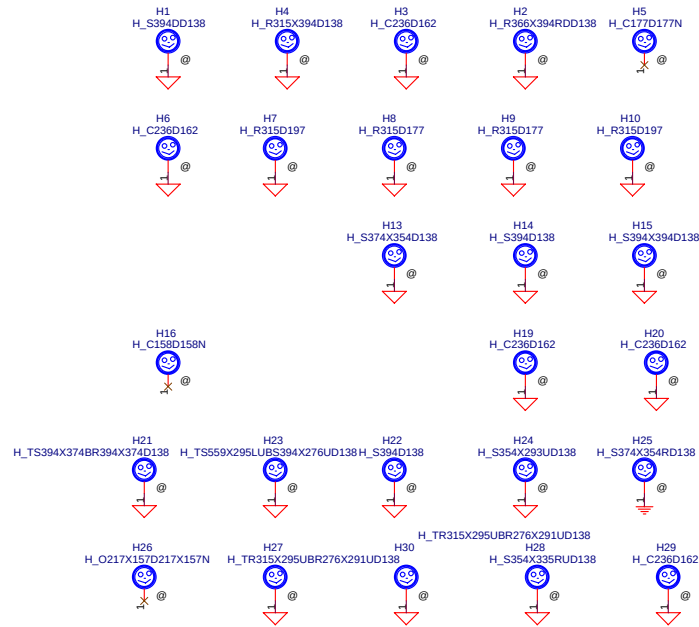
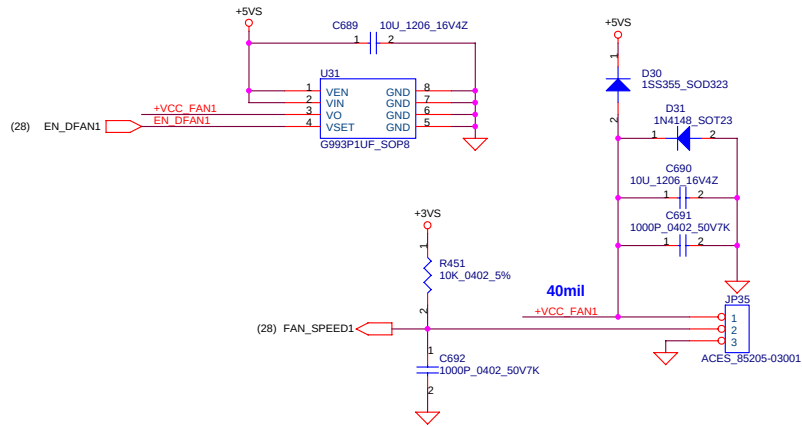


HD Audio Codec



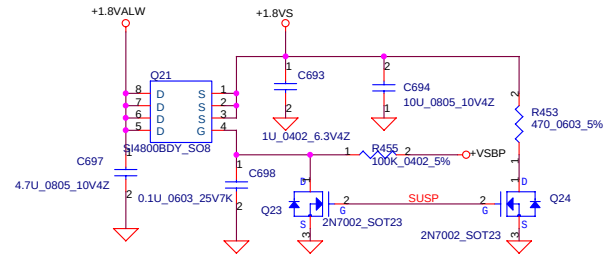
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FAN1 Conn

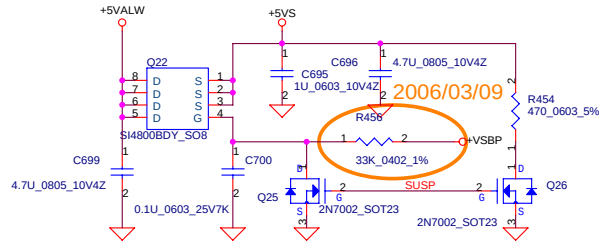


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+1.8VALW TO +1.8VS

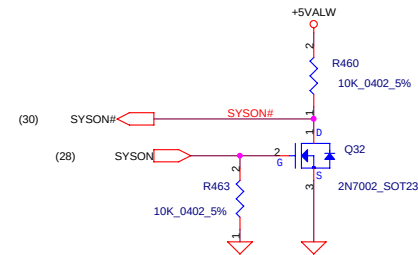
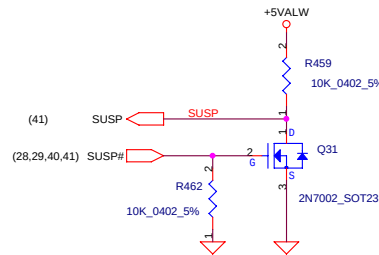
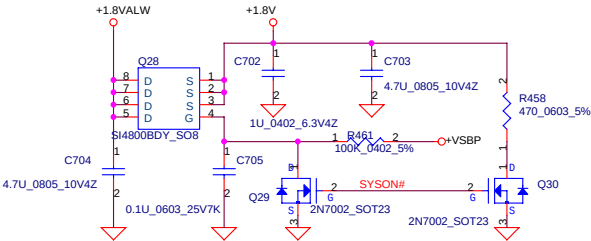


+5VALW TO +5VS

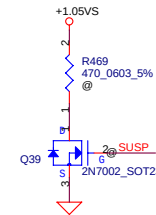
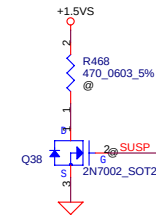
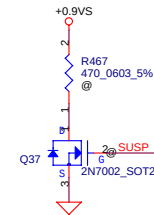
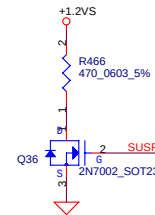
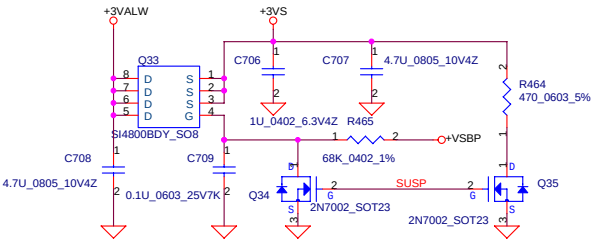


1207 DEL

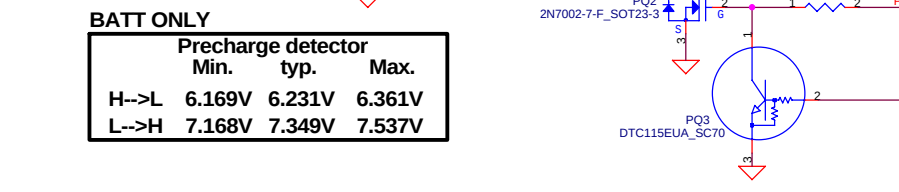
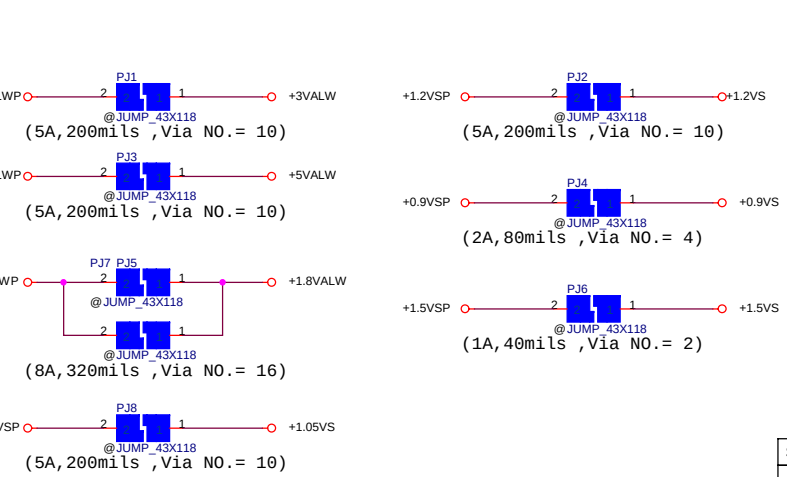
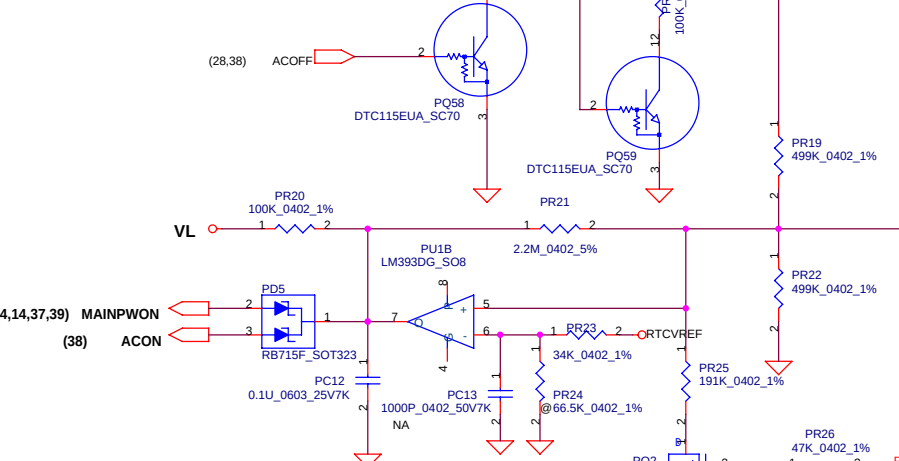
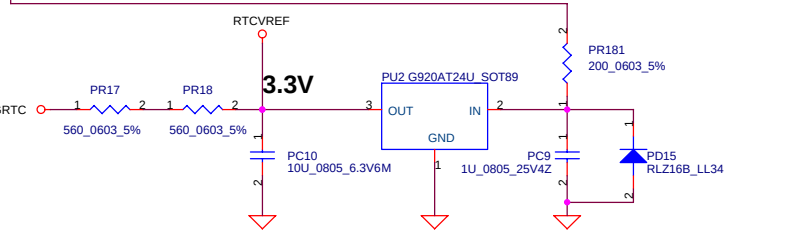
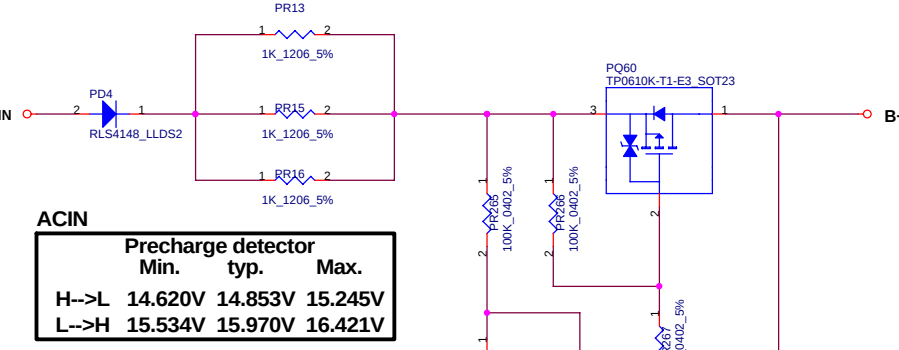
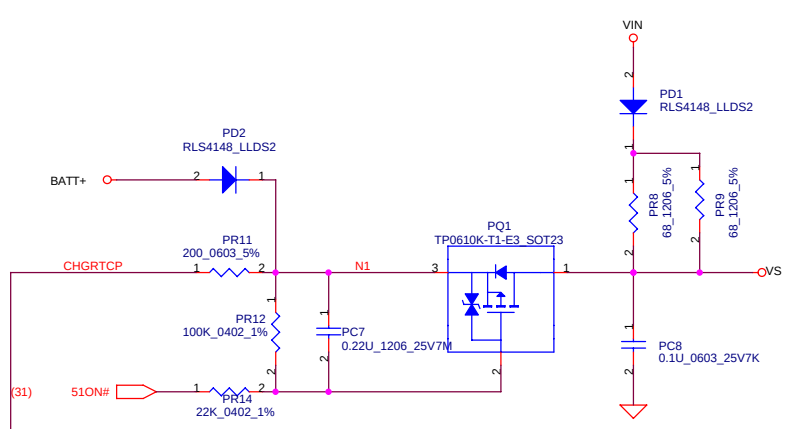
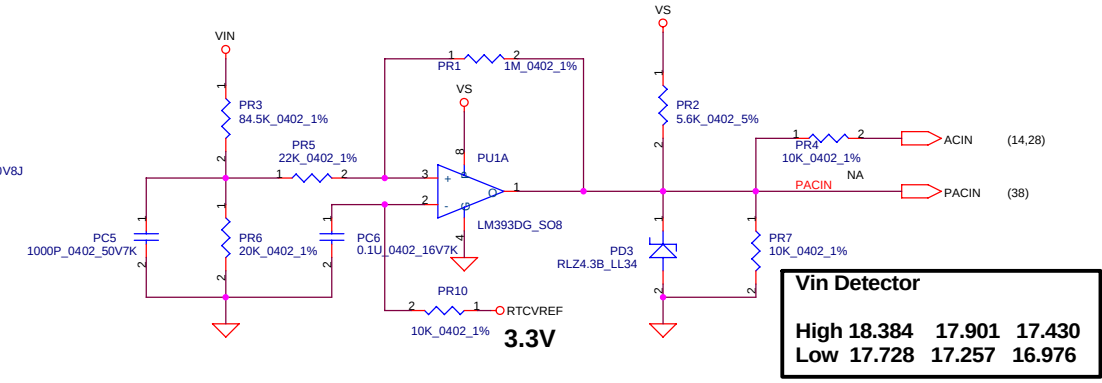
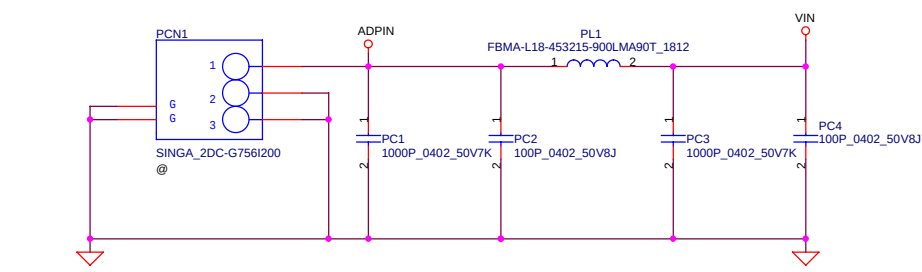
+1.8VALW TO +1.8V



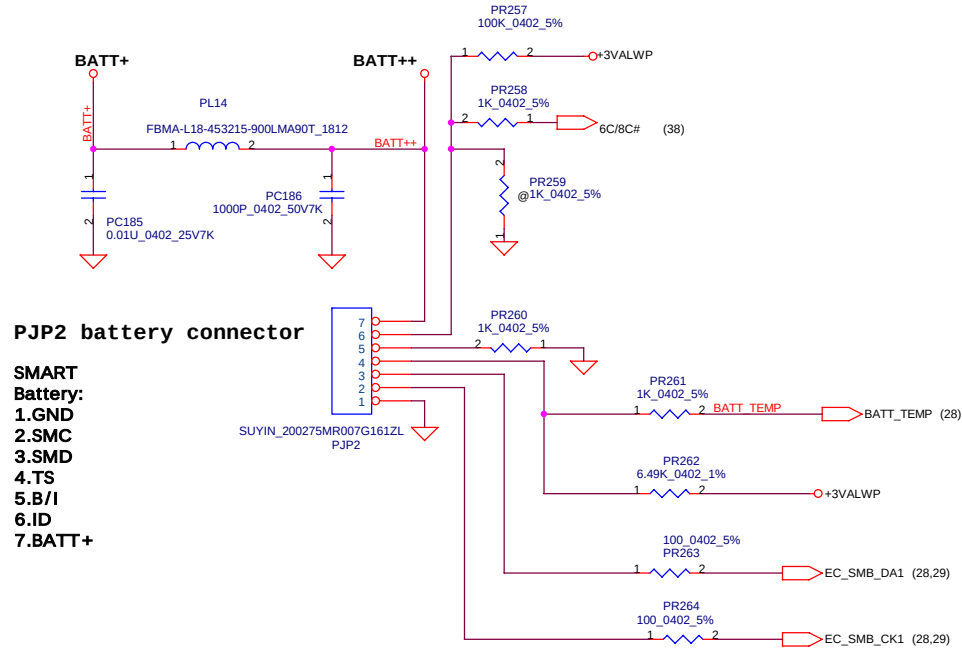
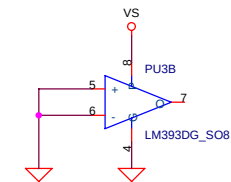
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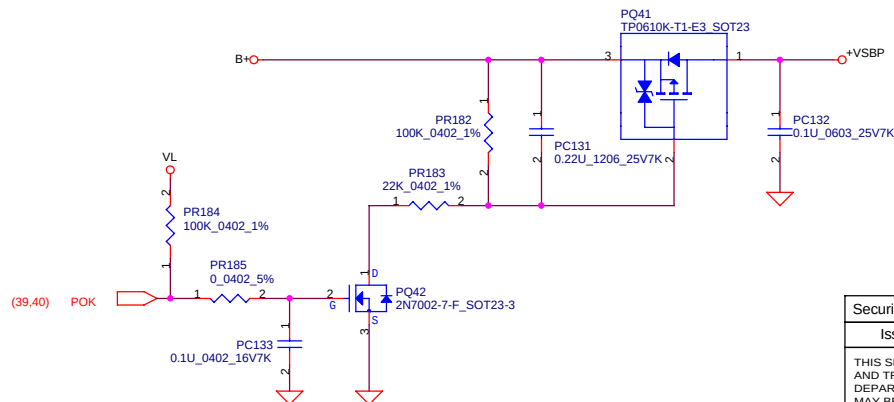
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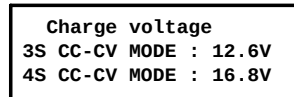
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Issued Date	2005/11/01	Deciphered Date	2006/11/30	Title
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**SMART
Battery:**
1.GND
2.SMC
3.SMD
4.TS
5.B/I
6.ID
7.BATT+



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LI-4S :17.8V---BATT-OVP=1.98V
BATT-OVP=0.111*BATT+
LI-3S :13.35V---BATT-OVP=1.98V
BATT-OVP=0.111*BATT+

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				Date	星期五 - 四月 11 2006	Sheet

+3.3VALWP/+5VALWP

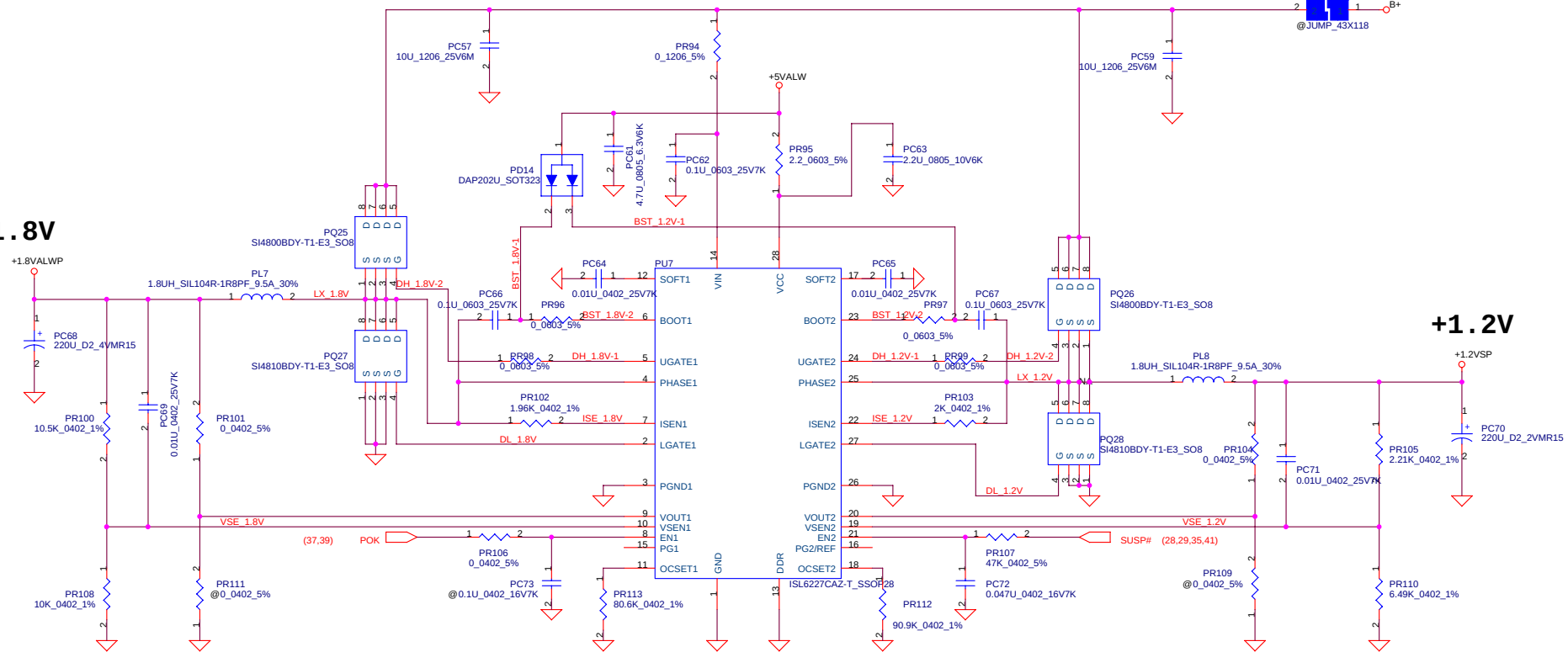
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Issued Date	2005/11/01	Deciphered Date	2006/11/30	Title	+5V/+3V	
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				Customer	0.4	
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+1.8VP O.C.P= 9.68A~15.72A

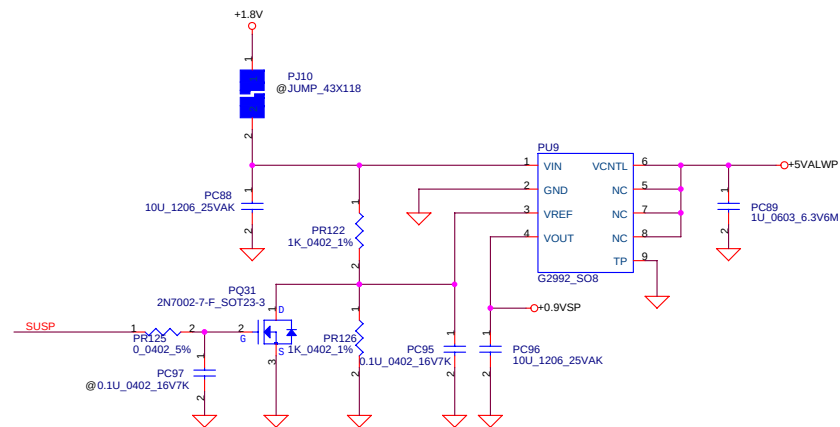
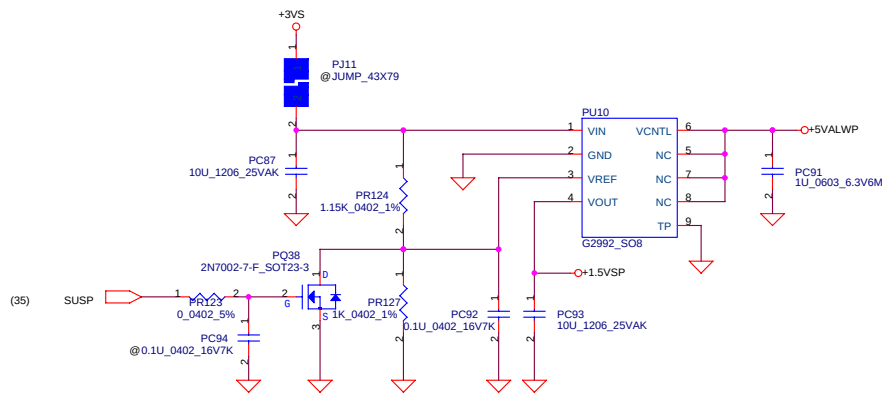
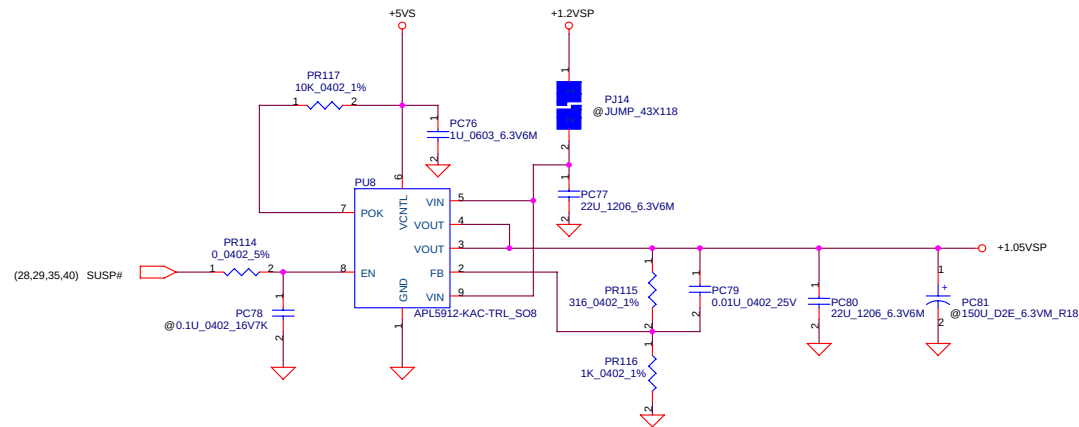
+1.2VP O.C.P= 8.67A~14.09A

+1.8V

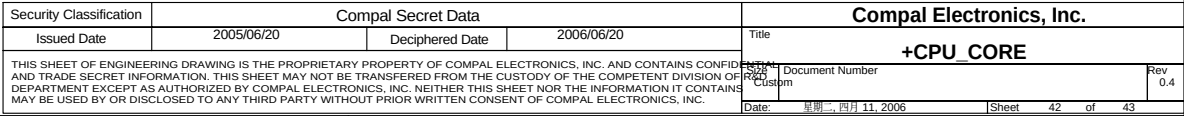
+1.2V



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Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	VER	Phase
1		For EMI require CPU core change from 0 to 2.2		42	MODIFY PR268/PR269 FROM 0 TO 2.2		DVT
2		modify 1.2V sequence(HW require)		40	change PR107 from 0 to 1k ;add PC72: :0.01uF		DVT
3		modify 1.2V sequence(HW require)		40	change PR107 from 1K to 47K ;change PC72: : from 0.01uF to 0.047uF		PVT
4							
5							
6							
7							
8							
9							
10							
11							
8							
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